

6.111 Final Report

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1 Abstract

Our project is about making a robot car that could track an object using a loaded camera, and move itself to follow the object. To make it simple, the object we used as were uni-color object/spheres, and color detection technique was used to track the object in the scene. Through VGA cables, the scene from the camera and visual feedback of the car motors were displayed on the screen to configure the parameters used to run the robot. Chase-bot will move to keep the object appear in the same location and the same size to keep the distance based on a control algorithm. By loading the FPGA, camera, batteries and all the other things necessary on the car, the robot is able to update the speeds of the motors at the frame rate of the camera which enables itself to track the object with minimum delay. Besides of the chasing task, we implemented another task using the same algorithm where the camera was attached to the side of the car and it would move only backward and forward to collide with the object, which we will refer to as the goal keeping task.

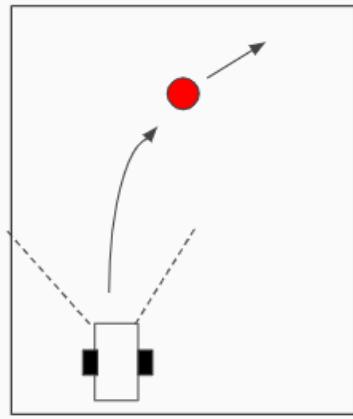


Figure 1: Chasing Task

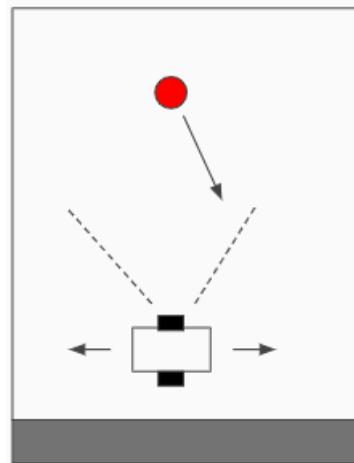


Figure 2: Goal Keeping Task

2 Project Goals

2.1 Baseline Goals

- Initialize the object to follow by a user interface with the camera input and a cursor on the screen
- Track the center and size of the object of interest using color detection

- Display a visual feedback of the tracking system showing which direction the car should move

2.2 Expected Goals

- Make the car chase the object by loading the camera in the front (Chasing Task)
- Make the car collide with the object by loading the camera on the side (Goal keeping)

2.3 Stretched Goals

- Make the car follow objects other than spheres
- Track itself using speed encoder
- Calculate real distance of the car and the object

3 System Design

3.1 High Level Block Diagram

The high level diagram of our system is shown in Figure 3. We have 3 major modules, tracker, controller, and initializer. The tracker module computes the radius and position of the tracking object, while the controller module generates adequate output to move the motor and drive the car. Initializer module deals with configuration of the object through visual interface and also takes care of the main FSM of this system since most of the states are related to initializing the object. The bram was used to store each frame when we display the camera input on the screen. It would lose 4 bit for each rgb due to capacity limitation. Although we needed to tune the parameters for tracking and controlling when debugging, we didn't have enough switches for that so we implemented a switch FSM which outputs the parameters based on the current switch values and the main state.

3.2 Main FSM

The main FSM of this system has 5 states. It starts with the initialize state where you choose which object to track by selecting a pixel (Figure 4) by moving the cursor using the buttons, and push the center button when necessary. After selection, it becomes the selected state, where the tracker would give the computed position and size on the screen as a white box. Then you can select it again to confirm you are satisfied with the tracking to move on the confirmed state. If you are not satisfied with the tracking, you could go back to initialize state by moving the cursor. The system would set the desired size of the object as the size of the object when you switch to confirmed state. The desired size

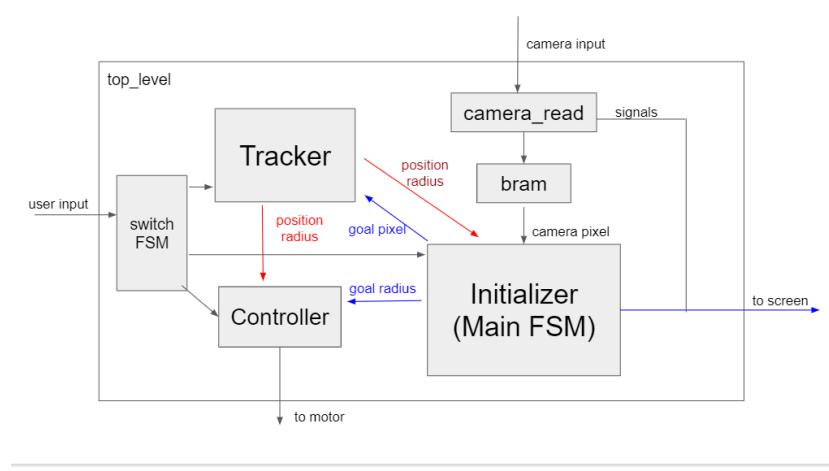


Figure 3: High level block diagram

corresponds to the distance between the car, so this transition would define how close the car would be to the object. In the confirmed state, the box would turn red, and there would be a visual feed back of the 2 motor outputs as 2 red bars on the right hand side of the screen.(Figure 5) The controller would compute the output for the motors, but it wouldn't actually output the signals since this state is for tuning the gains or setting the modes for control. Finally, when you are ready to move the car, you can deactivate the initializer to actually run! This is the move state, and you can always switch to pause mode where you can pause the car by pushing the center button.



Figure 4: initialize state



Figure 5: confirmed state

3.3 Hardware

2WD chassis

As the hardware of the robot, we used a 2 wheel driving chassis kit, which came with the body, 2 motors and wheels, battery box for the motor driver, and a passive wheel. Assembling the chassis was very straightforward. It was very intuitive with how to assemble the DC motors, wheels, and the battery box and solder the appropriate connections. Once the base of the chassis was assembled, the platform was installed by adding the motor driver at the bottom of the car (Figure 10) with wires connected to the battery box and the FPGA board loaded on the top side of the car. One issue that we had to confront was how to load all of the devices necessary on the limited space. This project required the FPGA, motor driver, battery pack for both motor driver and the camera all to be on the car. However, this platform was designed mainly in the use of Arduino where the board is quite smaller than Nexys 4 ddr. Therefore, we designed a second floor on the car using the acrylic plate and some spacers. This is quite similar to the FPGA stand in the 6.111 lab. As shown in Figure 7 the first floor had the battery pack for powering the FPGA and the FPGA was placed on the second floor. This provided enough area to fix the FPGA to the car in a stable manner and freedom to where the camera would be installed.

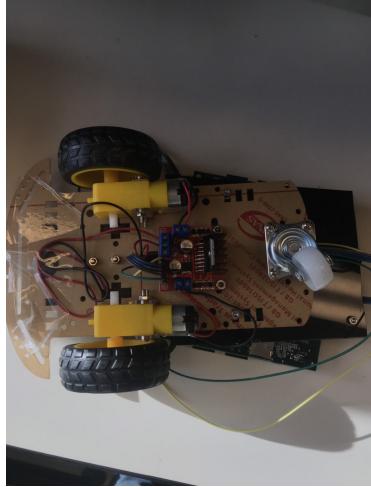


Figure 6: back view of the robot



Figure 7: overview of the robot

L298N motor driver

In order to drive the motor appropriately, there were 2 problems; first one is that the output voltage from the FPGA would be 3.3V, which would be not enough for moving the car and the second one is that we cannot control the speed because we cannot output analog voltage. The L298 is a high voltage,

high current dual full-bridge driver designed to accept not only DC motors but standard TTL logic levels and drive inductive loads such as relays, solenoids, and stepping motors. Two enable inputs were provided to enable or disable the motors independently of the input signals. L298N motor driver was used to amplify the voltage driven into the motors, and make it controllable using pulse width modulation (pwm) as the enable inputs. As shown in Figure 8, the width of the pulse, in other words the duty cycle, of the pwm would change the average voltage driven into each motors. The speed of the dc motors are proportional to the fed in voltage. Under the condition that the supply volatage was 6[V], the voltage would be described as

$$(DutyCycle) \times 6[V]$$

The circuit configuration of L298N is shown in Figure 9. Besides the enable input, there are 2 inputs, IN1 and IN2, to control the direction of each motor. Having IN1 high and IN1 low would drive the motor forward and vice versa.

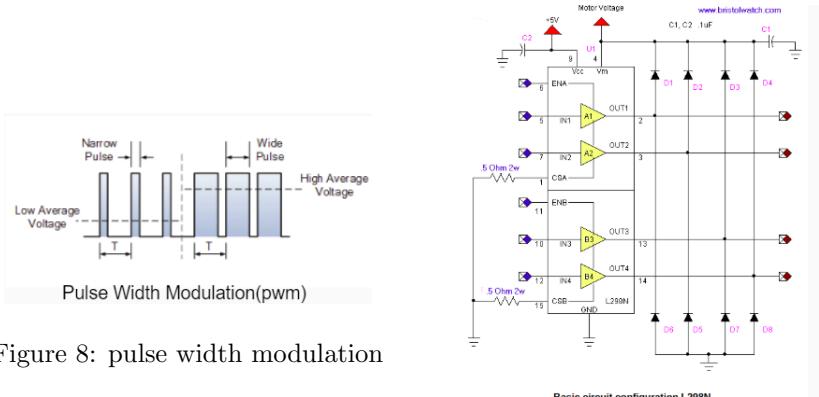


Figure 8: pulse width modulation

Figure 9: L298N circuit

OV7670 Camera

The camera we used was provided by the lab with arduino board for processing and some verilog codes useful for interfacing the camera. It had around 30 frame per seconds, each frame with 320*240 pixels. The ja and jb port of Nexys ddr 4 was occupied for camera interaction.

4 Modules

4.1 Tracker module [Emmanuel]

Tracker modules taken in a camera and color and outputs radius and position. A camera captures an image of the scene and that image is passed through

a color space conversion module which gives out an image in an easy to color detect format. That image is then passed through a color detector[hereby named threshold] which output the color when color in image match color of a selected pixel in initialization stage. After getting pixels that match the color, the xcenter and ycenter are computed by weighted sum and radius derived using number of pixels as area and then using square root and divider IP modules

$$x_{center} = \frac{\sum_0^n x_i}{n}$$

$$y_{center} = \frac{\sum_0^n y_i}{n}$$

$$radius = \sqrt{\frac{8 \times n}{22}}$$

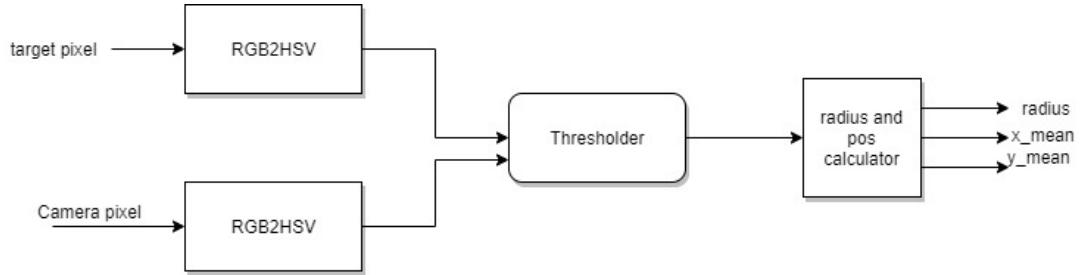


Figure 10: Block diagram of tracker module

for n pixels and x_i and y_i being the pixel locations of the detected object

RGB2HSV module

Since we are doing color detection and color detection in RGB is not optimal. we need a module to change RGB pixel to HSV and then color threshold in HSV. HSV module had a delay of about 22 clock cycles that we had to correct for in computing the radius, y and x positions of an object.

color_class module

to detect colors first attempt was to have a margin over a color of a pixel selected in initialization stage. But we realized that a one margin for all colors was not great as color bands are not equal and sample of the color may be selected near another color. so we need a color class module to classify a pixel and use that class in detection.

4.2 Initializer module [Shuto]

The initializer module took in buttons for cursor control and selection, position and radius of the object for generating the box, speed of two motors for displaying visual feedback of the motor, and other signals necessary for display. The outputs are the output pixel, goal pixel for tracker, goal radius for control, and the state. The module could be broken down to several subsystems.

State Transition

The state transition of our FSM was quite simple. The buttons for controlling the cursors and the activation switch were the only ones to trigger transition. Our car would only move at the move state, and other states are only for configuration or pausing.

debouncer

Since some state transition rely on user input buttons, noise is likely to ruin the FSM. The debouncer make sure the button is high for at least 10 ms to actually say that the button is pressed.

box

Using information of the position and radius of the object from the tracker module, generates the box to show what it tracks. The color is white during initialize and selected state, and red during the other states.

cursor

Generates the cursor for the user to select the object. The center position would move accordingly to the button inputs, at the speed of 2 pixels per frame. The cursor would only be displayed at initialize and selected state.

colorpad

Generates a $30 * 30$ blob in the color of the pixel of interest at the right bottom side of the screen. At the initialize state, it will display the color of the pixel at the center of the pixel, while in the other states, it will be the selected pixel instead. This allows access to which color that you are trying to track, which made debugging easier.

speed bar

Displays a visual feedback for the motor output on the right hand side of the screen. Consists of a horizontal base line and two red bars indicating the speed of each motor. Based on the 8 bit speed and forward/backward signals for each motors, the bar would be longer as the speed is higher and would face upwards if it is moving forward.

4.3 controller module [Shuto]

The controller module takes in the x,y position and the size of the object from the tracker module, and goal size of the object from the initializer module to generate signals to drive the motors properly based on control algorithm. This module has 4 subsystems.

control

This module uses a PD control algorithm to generate the speed of the car and how much it turns as a 9 bit signed value, based on the error in both x position and radius. The desired x was set as the center of the camera, while the desired radius was an input from the initializer. It also takes in 12 bits parameter for the gains for the control, and 2 bits parameter indicating which mode to be in. There are 3 modes, debugging, chasing, and goal keeping. In the debugging mode, the 12 bits parameter would be the direct output of this module. This mode was helpful to check if the hardware was really working or not. In the chasing mode, the 12 bit parameter was for the proportional and differential gain for both turning and speed, 3 bits each. The speed was obtained by the PD control for the radius of the object, and turning was obtained by the PD control for the x position of the object. Note that the gains take care of the converting pixel space x and radius into the proportional space speed and turn. Since the sample rate is constant, we just used the difference between the recent two frames for the differential. The control equations for the chasing task would be as below,

$$\begin{aligned} \text{speed} &= K_{sp}\tilde{r} + K_{sd}\delta\tilde{r} \\ \text{turn} &= K_{tp}\tilde{x} + K_{td}\delta\tilde{x} \end{aligned}$$

where

$$\begin{aligned} \tilde{r} &= r_{desired} - r \\ \tilde{x} &= x_{desired} - x \\ \delta\tilde{r} &= \tilde{r}_n - \tilde{r}_{n-1} \\ \delta\tilde{x} &= \tilde{x}_n - \tilde{x}_{n-1} \end{aligned}$$

In the goal keeping mode, the first 6 bits of the parameters was the proportional and differential gain for the x position. The radius information was not used since in this task the movement won't be affected by how close the object is. The control equations for this task would be as follows.

$$\text{speed} = K_{sp}\tilde{x} + K_{sd}\delta\tilde{x}$$

$$\text{turn} = 0$$

motor out

This module takes in the speed and the turning of the car and breaks that down into the speed and direction of two motors. We used a simple model for this, where the average speed of the 2 motors would be the overall speed of the car, and the turning would be the difference in the speed of 2 motors (Figure 11). In the real hardware, because of the weight of all the devices, the car would not move until it had enough voltage to beat the friction. In our case, the voltage seemed to be around 1.2V, so we added an offset of 1V equivalent value to the speeds we obtained with the model above. This turned out to be helpful to make the car become more sensitive to the object position.

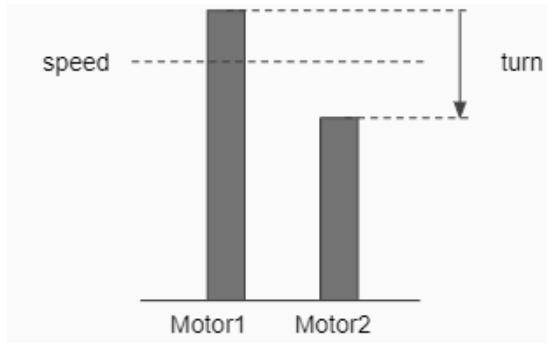


Figure 11: Conversion from car speed,turning to motor speed

After acquiring the speed and direction for both of the motors, this module generated the proper IN1,IN2, and enable signal for each using pwmgen below for the enable.

pwmgen

This module was used to generate the pwm based on the 8 bit input. We were able to generate 255 types of pwm signals in other words 255 types of speed for the motors.

xr_process

The estimated radius and x from the tracker module was noisy in that if the object was out of screen it reacted to the few pixel in the background and generated a bad radius and position. This caused the car to move randomly when it lost the object. Another problem was that since the camera angle was smaller than we expected, it was more likely to get out from the screen. This module took care of this 2 problems by pre-processing the radius and x from the tracker before it gets fed into the control. When the radius was too small, we estimated that the object was out of sight. We also made the car to move

just the way it was for 10-15 frames after it lost the object and stop. This made the chance of getting the object in the scene again higher after it lost it once.

5 Challenges

For the color detection, the resolution of the camera was 4bit for the processed signals. While normal cameras have 8 bit each color channel R,G,B our camera had 4—5. With less resolution it was hard to tell colors which are very similar. In terms of the design of the hardware, since the car was much more smaller than I had expected, figuring out a way to load everything was a challenge. By making it a two floor car, we were able to make it not only packed but also robust. One regret is that we couldn't think of a way to fix the camera for each task. Another challenge was that the car did not act the way I thought. One example was that the with all the devices on board the car had required some torque to start making it move. We dealt with that by adding offset voltage to the motor out module. The chasing task turned out to perform well, but we had to figure out how to overcome the weakness of having a limited camera angle. Holding the output for few frames after the car loses the object definitely helped, but it wasn't enough to make it follow an object crossing right in front of the car. We did not have time to explore better solutions for that. The hardest thing about the goal keeping task was that the car does not move straight even though the 2 motor voltages are the same. Having an encoder for feedback or manually tuning the turning effect might have helped, but we did not have the time.

6 Future Work

As mentioned in the challenges, using the encoder would broaden the options of what we can do next. For example, having a feedback system or self tracking would be possible. For a simple extension of the project, a better camera with large angle of view would definitely help make a better tracking system and a control system . Future teams can also include robust noise reduction and make a more a better object detector. For example our object detection relied solely on color of the object, but other teams can explore shape recognition by correlation in 2D and use of a cascade of morphological processes, and hopefully track non-generic object like human faces.

7 Conclusion & Advices

We were able to track objects with different colors, and made our robot do two tasks which were goalkeeping and following. Most our modules were independently testable which made integration easier at the end.

We initially spent a lot of time on rgb2hsv module confused about divider module. Asking help earlier probably would have saved sometime. For future

students, we recommend to integrate and start testing early. The first few iteration would never be perfect, so try testing and experimenting as early as you can. We believe that we were successful in that we set our goals doable, and had some time to improve the performance, but we still could have tested more and done more stretch goals.

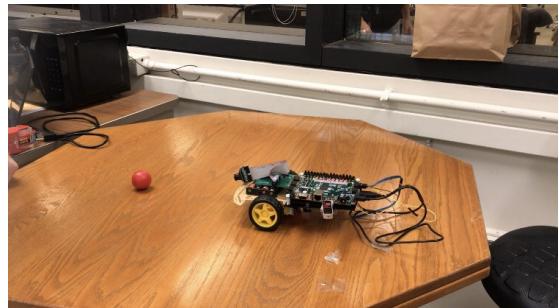


Figure 12: Chase-bot chasing a ball

A Appendix: Verilog Code

The code for the project can be found at <https://github.com/ehavugi/chasebot/tree/sources> sources branch have source files used.(we had issue with ip cores due to different vivado version). test1(a vivado project)

The list of modules

- track_init.sv
- tracker.sv
- rgb2hsv.sv
- blob.sv
- camera_read.sv
- control.sv
- xvga.sv
- clk_wiz_lab3.sv
- display_8hex.sv
- initialize.sv
- control.sv
- motor_out.sv
- color_class.sv

track_init.sv

```
1 `timescale 1ns / 1ps
2 //
3 // Company:
4 // Engineer:
5 //
6 // Create Date: 11/26/2019 05:42:29 PM
7 // Design Name:
8 // Module Name: track_init
9 // Project Name:
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
```

```

17 // Revision 0.01 - File 'timescale 1ns / 1ps
18 //
19 ///////////////////////////////////////////////////////////////////
20 // Updated 8/10/2019 Lab 3
21 // Updated 8/12/2018 V2.lab5c
22 // Create Date: 10/1/2015 V1.0
23 // Design Name:
24 // Module Name: labkit
25 //
26 //
27 ///////////////////////////////////////////////////////////////////
28 module track_init_control(
29     input clk_100mhz,
30     input [15:0] sw,
31     input btnc, btnu, btnl, btnr, btnd,
32     input [7:0] ja,
33     input [2:0] jb,
34     output jbclk,
35     input [2:0] jd,
36     output jdclk,
37     output [3:0] vga_r,
38     output [3:0] vga_b,
39     output [3:0] vga_g,
40     output vga_hs,
41     output vga_vs,
42     output led16_b, led16_g, led16_r,
43     output led17_b, led17_g, led17_r,
44     output[15:0] led,
45     output ca, cb, cc, cd, ce, cf, cg, dp, // segments a-g,
46             dp
47     output[7:0] an, // Display location 0-7
48     output[7:0] jc //for motor output
49 );
50     logic clk_65mhz;
51     // create 65mhz system clock, happens to match 1024 x
52         // 768 XVGA timing
53     clk_wiz_lab3 clkdivider(.clk_in1(clk_100mhz), .clk_out1(
54         clk_65mhz));
55     logic [31:0] data; // instantiate 7-segment
56         display; display (8) 4-bit hex
57     wire [6:0] segments;
58     assign {cg, cf, ce, cd, cc, cb, ca} = segments[6:0];
59     display_8hex display(.clk_in(clk_65mhz),.data_in(data),
60             .seg_out(segments), .strobe_out(an));
61     assign dp = 1'b1; // turn off the period

```

```

58
59     assign led = sw;
60
61     wire [10:0] hcount;      // pixel on current line
62     wire [9:0] vcount;       // line number
63     wire hsync, vsync, blank;
64     wire [11:0] pixel;
65     reg [11:0] rgb;
66     xvga xvga1(.vclock_in(clk_65mhz),.hcount_out(hcount),.
67                 vcount_out(vcount),
68                 .hsync_out(hsync),.vsync_out(vsync),.blank_out(
69                               blank));
70
71
72     // sw[0] button is user reset
73     wire reset;
74     debounce db1(.reset_in(reset),.clock_in(clk_65mhz),.
75                   noisy_in(sw[0]),.clean_out(reset));
76     logic scale; //1 when twice scaling
77
78     logic xclk;
79     logic[1:0] xclk_count;
80
81     logic pclk_buff, pclk_in;
82     logic vsync_buff, vsync_in;
83     logic href_buff, href_in;
84     logic[7:0] pixel_buff, pixel_in;
85
86     logic [11:0] cam;
87     logic [11:0] frame_buff_out;
88     logic [15:0] output_pixels; //pixel from camera
89     logic [12:0] processed_pixels; //stored inside bram
90     logic valid_pixel; //1 if inside camera frame
91     logic frame_done_out; //pulse indicating the end of
92                     frame
93
94     logic [16:0] pixel_addr_in;
95     logic [16:0] pixel_addr_out;
96
97     assign xclk = (xclk_count >2'b01);
98     assign jbclk = xclk;
99     assign jdclk = xclk;
100
101    blk_mem_gen_0 jojos_bram(.addra(pixel_addr_in),
102                             .clka(pclk_in),
103                             .dina(processed_pixels),
104                             .wea(valid_pixel),
105                             .addrb(pixel_addr_out),
106                             .clkb(clk_65mhz),
107                             .ena(1));

```

```

104                               .doutb(frame_buff_out));
105
106     always_ff @(posedge pclk_in)begin
107         if (frame_done_out)begin
108             pixel_addr_in <= 17'b0;
109         end else if (valid_pixel)begin
110             pixel_addr_in <= pixel_addr_in +1;
111         end
112     end
113
114     always_ff @(posedge clk_65mhz) begin
115         pclk_buff <= jb[0];//WAS JB
116         vsync_buff <= jb[1]; //WAS JB
117         href_buff <= jb[2]; //WAS JB
118         pixel_buff <= ja;
119         pclk_in <= pclk_buff;
120         vsync_in <= vsync_buff;
121         href_in <= href_buff;
122         pixel_in <= pixel_buff;
123         xclk_count <= xclk_count + 2'b01;
124         processed_pixels = {output_pixels[15:12],
125                             output_pixels[10:7],output_pixels[4:1]};
126
127
128         assign pixel_addr_out = scale?((hcount>>1)+(vcount>>1)
129                                         *32'd320):hcount+vcount*32'd320;
130         assign cam = scale&&((hcount<640) && (vcount<480))?
131                                         frame_buff_out:~scale&&((hcount<320) && (vcount<240)
132                                         )?frame_buff_out:12'h000;
133         assign {red,green,blue}=cam;
134
135
136         camera_read my_camera(.p_clock_in(pclk_in),
137                               .vsync_in(vsync_in),
138                               .href_in(href_in),
139                               .p_data_in(pixel_in),
140                               .pixel_data_out(output_pixels),
141                               .pixel_valid_out(valid_pixel),
142                               .frame_done_out(frame_done_out));
143
144         ////////////////////////////////for center positions and
145         ////////////////////////////////hsv/////////////////////////////
146         logic [23:0] radius;
147         logic [31:0] x_center,y_center;
148         logic [11:0] thres;
149         logic [11:0] pixel_out,goal_pixel,goal_rad;
150         logic [7:0] h_t,s_t,v_t;
151         logic show_thres,use_rgb;

```

```

149
150      rgb2hsv  goal_px(.clock(clk_65mhz),.reset(reset),.r({
151          goal_pixel[11:8],4'h0}),.g({goal_pixel[7:4],4'h0}), .
152          b({goal_pixel[3:0],4'h0}), .h(h_t), .s(s_t), .v(v_t))
153          ;
154
155      tracker my_tracker(
156          .clk(clk_65mhz),
157          .use_rgb(use_rgb),
158          .cam(cam),
159          .hcount(hcount),
160          .vcount(vcount),
161          .goalpixel(goal_pixel),
162          .vsync(vsync),
163          .radius(radius),
164          .x_center(x_center),
165          .y_center(y_center),
166          .thres(thres)
167      );
168
169
170
171
172
173
174
175
176
177
178
179
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181
182
183
184
185
186
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195
/////////////// INITIALIZE///////////////
logic signed [8:0] speed,turn;
logic en1,ina1,inb1,ina2,inb2,en2;
logic [7:0] speed_1,speed_2;
logic signed [8:0] speed1,speed2;
assign speed1 = {inb1,inb1?~speed_1 + 9'b1:speed_1};
assign speed2 = {inb2,inb2?~speed_2 + 9'b1:speed_2};

logic track,move;
logic [3:0] direction;
logic [2:0] state;
assign direction = {btnu,btnd,btnl,btnr};

initialize initializer(
    .clk_65mhz(clk_65mhz),
    .reset(reset),
    .hcount(hcount),
    .vcount(vcount),
    // .vsync(vsync_in),
    .vsync(frame_done_out),
    .directions(direction), //up,down,left,right
    .confirm_in(btnc),
    .activate_in(sw[1]),
    .sw2(scale), //whether to make the size twice
    .cam(show_thres?thres:cam),
    .cur_pos_x(x_center[8:0]),
    .cur_pos_y(y_center[8:0]),

```

```

196     .cur_rad(radius),
197     .speed1(speed1),
198     .speed2(speed2),
199     .pixel_out(pixel_out),
200     .goal_pixel(goal_pixel),
201     .goal_rad(goal_rad),
202     .track(track),
203     .move(move)
204     //for debug
205     ,
206     .state(state)
207     //      .cursor_x(cursor_x),
208     //      .cursor_y(cursor_y),
209     //      .up(dir[3]),
210     //      .down(dir[1]),
211     //      .left(dir[2]),
212     //      .right(dir[0])
213   );
214   /////////////////////////////////
215
216
217
218   ////////////////////CONTROL/////////////////
219   logic [3:0] Kps,Kpt;
220   logic [2:0] Kds,Kdt;
221   logic [1:0] mode;
222   logic [15:0] params;
223   logic [8:0] x,y;
224   logic [6:0] rad;
225   assign params = mode[1]?{Kps,Kds,Kpt,Kdt,mode}:{
226     speed1_in,speed2_in,mode};
227
228   assign x = &x_center?9'd160:x_center[8:0];
229   assign y = y_center[8:0];
230   assign rad = (radius<7'd10)?goal_rad:radius;
231
232   control my_control( .clk_in(clk_65mhz),
233                         .rst_in(reset),
234                         .ready_in(frame_done_out),
235                         .cur_pos_x(x),
236                         .cur_pos_y(y),
237                         .cur_rad(rad),
238                         .goal_rad(goal_rad),
239                         .params({Kps,Kds,Kpt,Kdt,mode}),
240                         .speed(speed),
241                         .turn(turn)
242   );
243
244   motor_out my_motor( .clk_in(clk_65mhz),
245                         .rst_in(reset),

```

```

245         .offset(8'd50),
246         .speed_in(speed),
247         .turn_in(turn),
248         .motor_out({en1,ina1,inb1,ina2,inb2,
249                     en2}),
250         .speed_1(speed_1),
251         .speed_2(speed_2)
252     );
253
254     assign jc[5:0] = move?{en1,en2,ina2,inb2,ina1,inb1}:6'b0
255     ;
256 ///////////////////////////////////////////////////////////////////
257
258 parameter INITIALIZE = 0;
259 parameter SELECTED = 1;
260 parameter CONFIRMED = 2;
261 parameter MOVE = 3;
262 parameter PAUSE = 4;
263
264 logic [1:0] seg_display;
265 logic [7:0] speed1_in; //signed
266 logic [7:0] speed2_in;
267
268 assign scale = 0; //no scaling
269 //assign mode[1] = 1;
270 assign Kps[3] = 0;
271 assign Kpt[3] = 0;
272 assign speed1_in[1:0] = 0;
273 assign speed2_in[1:0] = 0;
274
275 // things to display on a 7 segment displays
276 always_ff @(posedge clk_65mhz) begin
277     case (seg_display)
278         2'b00: data <= {7'b0,speed1,7'b0,speed2}; // 
279                     xxxx(center)xxxx(size)x(switch)
280         2'b01: data <= {7'b0,x,3'b0,y, {1'b0,state}}; 
281                     // display 0123456 + sw[3:0]
282         2'b10: data <= {{2'b0,goal_rad},{5'b0,state}}; 
283         2'b11: data <= {rad,{1'b0,state}}; 
284         default: data <= {x_center[15:0],y_center[11:0],
285                     {1'b0,state}}; 
286     endcase;
287 end
288
289
290 //switch controls

```

```

287 //sw[0] is always reset
288 //sw[1] is always used for state transition
289
290     always @(posedge clk_65mhz) begin
291         case(state)
292             INITIALIZE: begin
293                 seg_display <= sw[14:13];
294                 use_rgb <= sw[12];
295                 show_thres <= sw[15];
296                 end
297             SELECTED: begin
298                 seg_display <= sw[14:13];
299                 use_rgb <= sw[12];
300                 show_thres <= sw[15];
301                 //calibration related stuff too
302                 end
303             CONFIRMED: begin
304                 {Kps[2:0],Kds,Kpt[2:0],Kdt,mode} <= sw[15:2]
305                 ;
306                 speed1_in[7:2] <= sw[15:10];
307                 speed2_in[7:2] <= sw[9:4];
308                 end
309             PAUSE: begin
310                 {Kps[2:0],Kds,Kpt[2:0],Kdt,mode} <= sw[15:2]
311                 ;
312                 speed1_in[7:2] <= sw[15:10];
313                 speed2_in[7:2] <= sw[9:4];
314                 end
315             default: begin
316                 {Kps[2:0],Kds,Kpt[2:0],Kdt,mode} <= sw[15:2]
317                 ;
318                 speed1_in[7:2] <= sw[15:10];
319                 speed2_in[7:2] <= sw[9:4];
320             endcase
321         end
322
323
324
325
326     //what to display
327     reg b,hs,vs;
328
329     always_ff @(posedge clk_65mhz) begin
330         hs <= hsync;
331         vs <= vsync;
332         b <= blank;
333         rgb <= pixel_out;

```

```

334     end
335
336     // the following lines are required for the Nexys4 VGA
337     // circuit - do not change
337     assign vga_r = ~b ? rgb[11:8] : 0;
338     assign vga_g = ~b ? rgb[7:4] : 0;
339     assign vga_b = ~b ? rgb[3:0] : 0;
340
341     assign vga_hs = ~hs;
342     assign vga_vs = ~vs;
343
344 endmodule

```

tracker.sv

```

1  `timescale 1ns / 1ps
2  //
3  // Company: MIT 6.111
4  // Engineer: Emmanuel HAVUGIMANA
5  //
6  // Create Date: 01.12.2019 19:50:24
7  // Design Name:
8  // Module Name: tracker
9  // Project Name:
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //
21
22
23 module tracker(
24     input clk,
25     input use_rgb,
26     input [11:0] cam,
27     input [10:0] hcount,
28     input [9:0] vcount,
29     input [11:0] goalpixel,
30     input vsync,
31     output logic [23:0] radius,

```

```

32     output logic [31:0] x_center,
33     output logic [31:0] y_center,
34     output logic [11:0] thres
35   );
36
37 logic [7:0] h_t,s_t,v_t;
38
39 logic [31:0] x_remainder;
40 logic [31:0] y_remainder;
41 logic [31:0] x_remainder1;
42 logic [31:0] y_remainder;
43 logic clk_65mhz;
44 logic [31:0] pos_y_d;
45 logic [31:0] pos_x_d;
46 logic [31:0] size;
47 logic [31:0] size_d;
48 logic [31:0] size_;
49 logic [31:0] size__;
50
51 logic [31:0] pos_y;
52 logic [31:0] pos_y_;
53 logic [31:0] pos_x;
54 logic [31:0] pos_x_;
55 logic [31:0] pos_x_d;
56 logic [7:0] h,s,v;
57 logic [3:0] red,green, blue;
58 logic [23:0] radius_;
59 logic [31:0] pos_y_;
60 logic [26:0] count_f=0;
61 logic [31:0] square_r;
62 logic ready4;
63 logic ready2;
64 logic ready3;
65 logic ready1;
66 logic ready;
67 logic threshold;
68
69 assign size__=size_*3'd7;
70 assign clk_65mhz=clk;
71
72 //changed any pixel from rgb to hsv
73 rgb2hsv x(.clock(clk_65mhz),.reset(reset),.r({red,4'h0}), .
    g({green,4'h0}), .b({blue,4'h0}), .h(h), .s(s), .v(v));
74
75 // process goal pixel from rgb to hsv
76 rgb2hsv goal_px(.clock(clk_65mhz),.reset(reset),.r({
    goalpixel[11:8],4'h0}),.g({goalpixel[7:4],4'h0}), .b({
    goalpixel[3:0],4'h0}), .h(h_t), .s(s_t), .v(v_t));
77
78 assign {red,green,blue}=cam; // get camera components

```

```

79
80
81 //always @(posedge clk) begin
82 //    if (count_f<6500000) begin
83 //        count_f<=count_f+1;
84 //    end
85 //    else begin
86 //        count_f<=0;
87 //        size_<=size_d;
88 //        pos_x_<=pos_x_d;
89 //        pos_y_<=pos_y_d;
90 //        radius_<=radius;
91 //    end
92 //end
93
94 always @ (negedge vsync) begin
95     count_f<=0;
96     size_<=size_d;
97     pos_x_<=pos_x_d;
98     pos_y_<=pos_y_d;
99     radius_<=radius;
100 end
101
102 // get the radius given radius squared
103 sqrt uut (.aclk(clk_65mhz),
104             .s_axis_cartesian_tdata(square_r),
105             .s_axis_cartesian_tvalid(1),
106             .m_axis_dout_tdata(radius),
107             .m_axis_dout_tvalid(ready4)
108         );
109
110 // get radius squared vien area(size__)
111 divider32 square_xx(.s_axis_divisor_tdata(32'd22),
112                     .s_axis_divisor_tvalid(1),
113                     .s_axis_dividend_tdata(size__),
114                     .s_axis_dividend_tvalid(1),
115                     .aclk(clk_65mhz),
116                     .m_axis_dout_tdata({square_r,x_remainder1}),
117                     .m_axis_dout_tvalid(ready3));
118
119 // get x_mean given sum of pixels and number of pixels
120 divider32 center_xx(.s_axis_divisor_tdata(size_),
121                     .s_axis_divisor_tvalid(1),
122                     .s_axis_dividend_tdata(pos_x_),
123                     .s_axis_dividend_tvalid(1),
124                     .aclk(clk_65mhz),
125                     .m_axis_dout_tdata({x_center,x_remainder}),
126                     .m_axis_dout_tvalid(ready2));
127
128 // compute Y center given sum of y values of pixels and

```

```

        number of pixels,
129   divider32 center_yy(.s_axis_divisor_tdata(size_),
130                 .s_axis_divisor_tvalid(1),
131                 .s_axis_dividend_tdata(pos_y_),
132                 .s_axis_dividend_tvalid(1),
133                 .aclk(clk_65mhz),
134                 .m_axis_dout_tdata({y_center,y_remainder}),
135                 .m_axis_dout_tvalid(ready1));
136
137
138   always_comb begin
139     if (use_rgb) threshold=(red>(green+4))&&(red>(blue+4));
140     else threshold=(h<h_t+5)&&(s>s_t-20)&&(v>v_t-20);
141   end
142
143   parameter DELAY_SIZE=23;
144   reg [10:0] hcount_delay [DELAY_SIZE:0];
145   reg [9:0] vcount_delay [DELAY_SIZE:0];
146   reg vsync_delay [DELAY_SIZE:0];
147   reg [4:0] i;
148   parameter SEL_D=22;
149
150   always@(posedge clk_65mhz) begin
151     //delay the hcount and vcount signals 18 times
152     hcount_delay[0]<=hcount;
153     vcount_delay[0]<=vcount;
154     vsync_delay[0]<=vsync;
155
156   //    pixel_out_delay<=pixel_out;
157   for(i=1; i<DELAY_SIZE; i=i+1) begin
158     hcount_delay[i] <= hcount_delay[i-1];
159     vcount_delay[i] <= vcount_delay[i-1];
160     vsync_delay[i] <= vsync_delay[i-1];
161   end
162
163 end
164
165 always @ (posedge clk_65mhz) begin
166   if (threshold) begin
167     thres<=cam;
168     size<=size+1;
169     pos_x<=pos_x+hcount_delay[SEL_D]; // to use the
170       right values of hcount and vcount given delay of
171       rgb2hsv
172     pos_y<=pos_y+vcount_delay[SEL_D];
173   end
174   else begin thres=12'b0;end
175   if (vsync_delay[SEL_D]) begin
176     size_d<=size;
177     pos_x_d<=pos_x;

```

```

176           pos_y_d<=pos_y;
177       end
178   else begin size<=0;
179     pos_x<=0;
180     pos_y<=0;
181   end
182 end
183
184 endmodule


---


  rgb2hsv.sv
  1 'timescale 1ns / 1ps
  2 //
  ///////////////////////////////////////////////////////////////////
  3 // Company:
  4 // Engineer: Kevin Zheng Class of 2012
  5 //           Dept of Electrical Engineering & Computer
  //           Science
  6 //
  7 // Create Date:    18:45:01 11/10/2010
  8 // Design Name:
  9 // Module Name:   rgb2hsv
 10 // Project Name:
 11 // Target Devices:
 12 // Tool versions:
 13 // Description:
 14 //
 15 // Dependencies:
 16 //
 17 // Revision:
 18 // Revision 0.01 - File Created
 19 // Additional Comments:
 20 //
 21 //
  ///////////////////////////////////////////////////////////////////
 22 module rgb2hsv(clock, reset, r, g, b, h, s, v);
 23   input wire clock;
 24   input wire reset;
 25   input wire [7:0] r;
 26   input wire [7:0] g;
 27   input wire [7:0] b;
 28   output reg [7:0] h;
 29   output reg [7:0] s;
 30   output reg [7:0] v;
 31   reg [7:0] my_r_delay1, my_g_delay1,
  //           my_b_delay1;
 32   reg [7:0] my_r_delay2, my_g_delay2,
  //           my_b_delay2;

```

```

33         reg [7:0] my_r, my_g, my_b;
34         reg [7:0] min, max, delta;
35         reg [15:0] s_top;
36         reg [15:0] s_bottom;
37         reg [15:0] h_top;
38         reg [15:0] h_bottom;
39         wire [15:0] s_quotient;
40         wire [15:0] s_remainder;
41         wire s_rfd;
42         wire [15:0] h_quotient;
43         wire [15:0] h_remainder;
44         wire h_rfd;
45         reg [7:0] v_delay [19:0];
46         reg [18:0] h_negative;
47         reg [15:0] h_add [18:0];
48         reg [4:0] i;
49         // Clocks 4-18: perform all the divisions
50         //the s_divider (16/16) has delay 18
51         //the hue_div (16/16) has delay 18
52
53
54     logic start;
55     parameter m=8;
56     reg[3:1] state=0;
57     assign start=1'b1;
58     reg[5:0] count=0;
59
60
61     div_gen_1 hue1(.aclk(clock),
62                   .s_axis_divisor_tvalid(1'b1),
63                   .s_axis_divisor_tdata(s_bottom),
64                   .s_axis_dividend_tvalid(1'b1),
65                   .s_axis_dividend_tdata(s_top),
66                   .m_axis_dout_tdata(s_quotient),
67                   .m_axis_dout_tvalid(s_rfd));
68
69     div_gen_1 hue2(.aclk(clock),
70                   .s_axis_divisor_tvalid(1'b1),
71                   .s_axis_divisor_tdata(h_bottom),
72                   .s_axis_dividend_tvalid(1'b1),
73                   .s_axis_dividend_tdata(h_top),
74                   .m_axis_dout_tdata(h_quotient),
75                   .m_axis_dout_tvalid(h_rfd));
76
77
78
79     always @ (posedge clock) begin
80
81         // Clock 1: latch the inputs (always positive)
82         {my_r, my_g, my_b} <= {r, g, b};

```

```

83
84 // Clock 2: compute min, max
85 {my_r_delay1, my_g_delay1, my_b_delay1} <= {my_r, my_g, my_b
86     };
87 if((my_r >= my_g) && (my_r >= my_b)) //(B,S,S)
88     max <= my_r;
89 else if((my_g >= my_r) && (my_g >= my_b)) //(S,B,S)
90     max <= my_g;
91 else
92     max <= my_b;
93
94 if((my_r <= my_g) && (my_r <= my_b)) //(S,B,B)
95     min <= my_r;
96 else if((my_g <= my_r) && (my_g <= my_b)) //(B,S,B)
97     min <= my_g;
98 else
99     min <= my_b;
100
101 // Clock 3: compute the delta
102 {my_r_delay2, my_g_delay2, my_b_delay2} <= {my_r_delay1,
103     my_g_delay1, my_b_delay1};
104 v_delay[0] <= max;
105 delta <= max - min;
106
107
108
109 if(my_r_delay2 == v_delay[0]) begin
110     h_top <= (my_g_delay2 >= my_b_delay2)?
111         (my_g_delay2 - my_b_delay2) * 8'd255:
112         (my_b_delay2 - my_g_delay2) * 8'd255;
113     h_negative[0] <= (my_g_delay2 >= my_b_delay2)?0:1;
114     h_add[0] <= 16'd0;
115 end
116 else if(my_g_delay2 == v_delay[0]) begin
117     h_top <= (my_b_delay2 >= my_r_delay2)?
118         (my_b_delay2 - my_r_delay2) * 8'd255:
119         (my_r_delay2 - my_b_delay2) * 8'd255;
120     h_negative[0] <= (my_b_delay2 >= my_r_delay2)?0:1;
121     h_add[0] <= 16'd85;
122 end
123 else if(my_b_delay2 == v_delay[0]) begin
124     h_top <= (my_r_delay2 >= my_g_delay2)?
125         (my_r_delay2 - my_g_delay2) * 8'd255:
126         (my_g_delay2 - my_r_delay2) * 8'd255;
127     h_negative[0] <= (my_r_delay2 >= my_g_delay2)?0:1;
128             h_add[0] <= 16'd170;
129 end

```

```

130
131          h_bottom <= (delta > 0)?delta * 8'd6
132                      :16'd6;
133
134          //delay the v and h_negative signals
135          // 18 times
136          for(i=1; i<19; i=i+1) begin
137              v_delay[i] <= v_delay[i-1];
138              h_negative[i] <= h_negative[
139                  i-1];
140              h_add[i] <= h_add[i-1];
141
142      end
143
144      v_delay[19] <= v_delay[18];
145      //Clock 22: compute the final value of h
146      //depending on the value of h_delay[18],
147      //we need to subtract 255 from it to make it come back
148      //around the circle
149      if(h_negative[18] && (h_quotient > h_add[18])) begin
150          h <= 8'd255 - h_quotient[7:0] + h_add[18];
151      end
152      else if(h_negative[18]) begin
153          h <= h_add[18] - h_quotient[7:0];
154      end
155      else begin
156          h <= h_quotient[7:0] + h_add[18];
157      end
158
159  endmodule

```

blob.sv

```

1  //////////////////////////////////////////////////////////////////
2  //
3  // blob: generate rectangle on screen
4  //
5  //////////////////////////////////////////////////////////////////
6  module blob
7      #(parameter COLOR = 12'hFFF) // default color: white
8      (input [10:0] x_in,hcount_in,
9       input [9:0] y_in,vcount_in,
10      input [7:0] width,height,

```

```

11     output logic [11:0] pixel_out);
12
13     always_comb begin
14         if ((hcount_in >= x_in && hcount_in < (x_in+width)) &&
15             (vcount_in >= y_in && vcount_in < (y_in+height)))
16             pixel_out = COLOR;
17         else pixel_out = 0;
18     end
19 endmodule
20
21
22 module box
23     #(parameter THICKNESS = 2,
24      COLOR = 12'hFFF) // default color: white
25     (input [10:0] x_in,hcount_in,
26      input [9:0] y_in,vcount_in,
27      input [7:0] radius_in,
28      output logic [11:0] pixel_out);
29
30     logic [6:0] inner; //length to specify inside the box
31     assign inner = radius_in - THICKNESS;
32
33 //asssuming the ball is always fully inside the picture
34     always_comb begin
35         //if inside outside frame
36         if ((hcount_in >= (x_in-radius_in) && hcount_in < (
37             x_in+radius_in)) &&
38             (vcount_in >= (y_in-radius_in) && vcount_in < (y_in
39                 +radius_in))) begin
40                 //if outside inside frame
41                 if (~(hcount_in >= (x_in-inner) && hcount_in
42                     < (x_in+inner)) |
43                     ~(vcount_in >= (y_in-inner) && vcount_in
44                         < (y_in+inner))) begin
45                     pixel_out = COLOR;
46                 end
47                 else pixel_out = 0;
48             end
49         else pixel_out = 0;
50     end
51 endmodule
52
53 module cursor
54     #(parameter THICKNESS = 1,
55      COLOR = 12'hFFF, // default color: white
56      WIDTH = 320, //display width
57      HEIGHT = 240 //display height
58      )
59     (input [10:0] x_in,hcount_in,
60      input [9:0] y_in,vcount_in,

```

```

57     input  sw2,
58     output logic [11:0] pixel_out);
59
60     always_comb begin
61         if (~sw2) begin
62             if ((hcount_in <= WIDTH && vcount_in == y_in) |
63                 (vcount_in <= HEIGHT && hcount_in == x_in))
64                 pixel_out = COLOR;
65             else pixel_out = 0;
66         end
67         else begin
68             if ((hcount_in <= WIDTH*2 && vcount_in == y_in) |
69                 (vcount_in <= HEIGHT*2 && hcount_in == x_in))
70                 pixel_out = COLOR;
71             else pixel_out = 0;
72         end
73     end
74 endmodule
75
76
77 module colorpad
78     #(parameter WIDTH = 30,      //pad width
79                  HEIGHT = 30,      //pad height
80                  X = 800,        //pad x
81                  Y = 600,        //pad y
82                  )
83     (input [10:0] hcount_in,
84      input [9:0] vcount_in,
85      input [11:0] pixel_in,
86      output logic [11:0] pixel_out);
87
88     always_comb begin
89         if ((hcount_in >= X && hcount_in < (X+WIDTH)) && (
90             vcount_in >= Y && vcount_in < (Y+HEIGHT)))
91             pixel_out = pixel_in;
92         else pixel_out = 0;
93     end
94 endmodule
95
96
97 module speed_bar //display a bar indicating speed of each
98     motor
99     #(parameter WIDTH=50, //length of the bar
100      HEIGHT =256, //height of the bar
101      X = 700, //start pos
102      Y = 300, //baseline pos
103      TOTAL = WIDTH*5,
104      COLOR = 12'hF00 // default color: red, the

```

```

                                baseline is white
100
101      )
102      (input [10:0] hcount_in,
103      input [9:0] vcount_in,
104      input signed [8:0] speed1,speed2,
105      output logic [11:0] pixel_out);
106
107      logic [10:0] x1,x2;
108      logic [9:0] y1,y2;
109      logic [11:0] motor1,motor2,bar;
110      logic [7:0] abs1,abs2;
111
112      assign x1 = X + WIDTH;
113      assign x2 = X + WIDTH*3;
114      assign y1 = speed1[8]?Y:Y-speed1[7:0];
115      assign y2 = speed2[8]?Y:Y-speed2[7:0];
116      assign abs1 = speed1[8]?~speed1[7:0]+8'b1:speed1[7:0];
117      assign abs2 = speed2[8]?~speed2[7:0]+8'b1:speed2[7:0];
118
119 //      assign pixel_out = &bar?bar:motor1 + motor2;
120      assign pixel_out = motor1;
121      blob #(.COLOR(COLOR)) m1
122          (.x_in(x1), .y_in(y1), .hcount_in(hcount_in), .
123              vcount_in(vcount_in), .width(WIDTH), .height(
124                  abs1), .pixel_out(motor1));
125      blob #(.COLOR(COLOR)) m2
126          (.x_in(x2), .y_in(y2), .hcount_in(hcount_in), .
127              vcount_in(vcount_in), .width(WIDTH), .height(
128                  abs2), .pixel_out(motor2));
129
130 endmodule
131
132 module arrow //To be continued
133     #(parameter WIDTH=50, //length of the bar
134             HEIGHT =256, //height of the bar
135             X = 800, //start pos
136             Y = 200, //baseline pos
137             TOTAL = WIDTH*5,
138             COLOR = 12'hFOO // default color: red, the
139                 baseline is white
140             )
141     (input [10:0] hcount_in,
142     input [9:0] vcount_in,

```

```

142      input signed [8:0] speed1,speed2,
143      output logic [11:0] pixel_out);
144
145 endmodule

```

```

camera_read.sv

1 module camera_read(
2     input p_clock_in,
3     input vsync_in,
4     input href_in,
5     input [7:0] p_data_in,
6     output logic [15:0] pixel_data_out,
7     output logic pixel_valid_out,
8     output logic frame_done_out
9 );
10
11     rgb2hsv xx(.clock(), .reset(), .r(), .g(), .b(), .h
12         (),.s(), .v());///
13     logic [1:0] FSM_state = 0;
14     logic pixel_half = 0;
15
16     localparam WAIT_FRAME_START = 0;
17     localparam ROW_CAPTURE = 1;
18
19     always_ff@(posedge p_clock_in)
20     begin
21         case(FSM_state)
22
23             WAIT_FRAME_START: begin //wait for VSYNC
24                 FSM_state <= (!vsync_in) ? ROW_CAPTURE :
25                     WAIT_FRAME_START;
26                 frame_done_out <= 0;
27                 pixel_half <= 0;
28             end
29
30             ROW_CAPTURE: begin
31                 FSM_state <= vsync_in ? WAIT_FRAME_START :
32                     ROW_CAPTURE;
33                 frame_done_out <= vsync_in ? 1 : 0;
34                 pixel_valid_out <= (href_in && pixel_half) ? 1 :
35                     0;
36                 if (href_in) begin
37                     pixel_half <= ~ pixel_half;
38                     if (pixel_half) pixel_data_out[7:0] <=
39                         p_data_in;
40                     else pixel_data_out[15:8] <= p_data_in;
41                 end
42             end
43         endcase

```

```

40         end
41
42 endmodule


---


control.sv
1 `timescale 1ns / 1ps
2
3
4 module control(
5             input clk_in,
6             input rst_in,
7             input ready_in,
8             input [8:0] cur_pos_x,
9             input [8:0] cur_pos_y,
10            input [6:0] cur_rad,
11            input [6:0] goal_rad,
12            input [15:0] params,
13            output logic signed [8:0] speed,
14            output logic signed [8:0] turn
15 );
16
17 //camera size
18 parameter HEIGHT = 240;
19 parameter WIDTH = 320;
20
21 //modes
22 parameter FORWARD = 0;
23 parameter DIRECT = 1;
24 parameter GOALKEEP = 3;
25 parameter CHASE = 2;
26
27 //assign params
28 logic signed [4:0] Ksp;
29 logic signed [3:0] Ksd;
30 logic signed [4:0] Ktp;
31 logic signed [3:0] Ktd;
32 logic [1:0] mode;
33
34 assign {Ksp[3:0],Ksd[2:0],Ktp[3:0],Ktd[2:0],mode} = params;
35
36 assign Ksp[4] = 0;
37 assign Ksd[3] = 0;
38 assign Ktp[4] = 0;
39 assign Ktd[3] = 0;
40
41 //desired x,r
42 logic [8:0] x_d;
43 logic [6:0] r_d;
44 assign x_d = WIDTH >> 1;
45 assign r_d = goal_rad;

```

```

46
47 //current x,rad,dx,dr
48 logic [8:0] x;
49 logic [6:0] r;
50 logic [8:0] dx;
51 logic [6:0] dr;
52
53 //previous x,rad,dx,dr
54 logic [8:0] pre_x;
55 logic [6:0] pre_r;
56 logic [8:0] pre_dx;
57 logic [6:0] pre_dr;
58
59
60 //errors
61 logic signed [8:0] e_x;
62 logic signed [8:0] e_r;
63 logic signed [8:0] e_dx;
64 logic signed [8:0] e_dr;
65
66 assign e_x = x_d - x; //abs less than 240
67 assign e_r = r_d - r;
68
69
70 //raw speed,turn
71 logic signed [16:0] raw_speed;
72 logic signed [16:0] raw_turn;
73
74
75 //threshold the output
76 logic [7:0] pass1;
77 logic [7:0] pass2;
78
79 threshold_by_abs threshold_speed(.signed_in(raw_speed), .
    threshold(16'h00ff), .signed_out({speed[8],pass1,speed[7:
    0]}));
80 threshold_by_abs threshold_turn(.signed_in(raw_turn), .
    threshold(16'h00ff), .signed_out({turn[8],pass2,turn[7:0]
    }));
```

81

82

83

84 always_comb begin

85 case(mode)

86 GOALKEEP:begin

87 raw_speed = (Ksp * e_x) + (Ksd * e_dx);

88 raw_turn = 0;

89 end

90 CHASE: begin

```

92                     raw_speed = (Ksp * e_r) + (Ksd * e_dr);
93                     raw_turn = (Ktp * e_x) + (Ktd * e_dx);
94             end
95         DIRECT: begin
96             raw_speed = {params[15],8'd0,params[14:8]
97                         ,1'b0};
98             raw_turn = {params[7],8'd0,params[6:0],1'
99                         b0};
100            end
101        default:begin
102            raw_speed = 0;
103            raw_turn = 0;
104        end
105    endcase
106 end
107
108 always_ff @(posedge clk_in) begin
109     if(rst_in) begin
110         //initialize
111         x <= 0;
112         r <= 0;
113         dx <= 0;
114         dr <= 0;
115         pre_x <= 0;
116         pre_r <= 0;
117         pre_dx <= 0;
118         pre_dr <= 0;
119     end
120     else begin
121         if(ready_in) begin
122             x <= cur_pos_x;
123             r <= cur_rad;
124             e_dx <= x - cur_pos_x;
125             e_dr <= r - cur_rad;
126         end
127     end
128 endmodule
129
130
131 module threshold_by_abs(
132     input signed [16:0] signed_in,
133     input [15:0] threshold,
134     output signed [16:0] signed_out
135 );
136
137 logic sign;
138 logic [15:0] abs;

```

```

140
141 assign sign = signed_in[16];
142 assign signed_out[16] = sign;
143
144 assign abs = sign?~signed_in[15:0] + 16'h0001:signed_in[15:0
    ];
145 assign signed_out[15:0] = (abs <= threshold)? signed_in[15:0
    ]:(sign?~threshold+16'h0001:threshold);
146 endmodule


---


xvga.sv
1
2
3 ///////////////////////////////////////////////////////////////////
4 // Update: 8/8/2019 GH
5 // Create Date: 10/02/2015 02:05:19 AM
6 // Module Name: xvga
7 //
8 // xvga: Generate VGA display signals (1024 x 768 @ 60Hz)
9 //
10 //                                     ----- HORIZONTAL -----
11 //                                     -----VERTICAL -----
12 //                                     Active
13 //                                     Active
14 //                                     Freq
15 //                                     Video   FP   Sync   BP
16 //                                     640x480, 60Hz 25.175 640    16    96    48
17 //                                     480     11    2     31
18 //                                     800x600, 60Hz 40.000 800    40   128    88
19 //                                     600     1     4     23
20 //                                     1024x768, 60Hz 65.000 1024   24   136   160
21 //                                     768     3     6     29
22 //                                     1280x1024, 60Hz 108.00 1280   48   112   248
23 //                                     768     1     3     38
24 //                                     1280x720p 60Hz 75.25 1280   72    80   216
25 //                                     720     3     5     30
26 //                                     1920x1080 60Hz 148.5 1920   88    44   148
27 //                                     1080    4     5     36
28 //
29 // change the clock frequency, front porches, sync's, and
30 // back porches to create
31 // other screen resolutions
32 //
33 ///////////////////////////////////////////////////////////////////
34 module xvga(input vclock_in,
35             output reg [10:0] hcount_out,      // pixel number

```

```

          on current line
26      output reg [9:0] vcount_out,      // line number
27      output reg vsync_out, hsync_out,
28      output reg blank_out);
29
30  parameter DISPLAY_WIDTH  = 1024;      // display width
31  parameter DISPLAY_HEIGHT = 768;       // number of lines
32
33  parameter H_FP = 24;                  // horizontal front
   porch
34  parameter H_SYNC_PULSE = 136;        // horizontal sync
35  parameter H_BP = 160;                // horizontal back
   porch
36
37  parameter V_FP = 3;                  // vertical front
   porch
38  parameter V_SYNC_PULSE = 6;          // vertical sync
39  parameter V_BP = 29;                // vertical back
   porch
40
41 // horizontal: 1344 pixels total
42 // display 1024 pixels per line
43 reg hblank,vblank;
44 wire hsyncon,hsyncoff,hreset,hblankon;
45 assign hblankon = (hcount_out == (DISPLAY_WIDTH -1));
46 assign hsyncon = (hcount_out == (DISPLAY_WIDTH + H_FP -
   1)); //1047
47 assign hsyncoff = (hcount_out == (DISPLAY_WIDTH + H_FP +
   H_SYNC_PULSE - 1)); // 1183
48 assign hreset = (hcount_out == (DISPLAY_WIDTH + H_FP +
   H_SYNC_PULSE + H_BP - 1)); //1343
49
50 // vertical: 806 lines total
51 // display 768 lines
52 wire vsyncon,vsyncoff,vreset,vblankon;
53 assign vblankon = hreset & (vcount_out == (DISPLAY_HEIGHT
   - 1)); // 767
54 assign vsyncon = hreset & (vcount_out == (DISPLAY_HEIGHT
   + V_FP - 1)); // 771
55 assign vsyncoff = hreset & (vcount_out == (DISPLAY_HEIGHT
   + V_FP + V_SYNC_PULSE - 1)); // 777
56 assign vreset = hreset & (vcount_out == (DISPLAY_HEIGHT +
   V_FP + V_SYNC_PULSE + V_BP - 1)); // 805
57
58 // sync and blanking
59 wire next_hblank,next_vblank;
60 assign next_hblank = hreset ? 0 : hblankon ? 1 : hblank;
61 assign next_vblank = vreset ? 0 : vblankon ? 1 : vblank;
62 always_ff @(posedge vclock_in) begin
63     hcount_out <= hreset ? 0 : hcount_out + 1;

```

```

64      hblank <= next_hblank;
65      hsync_out <= hsyncon ? 0 : hsyncoff ? 1 : hsync_out;
66          // active low
67
68      vcount_out <= hreset ? (vreset ? 0 : vcount_out + 1) :
69          vcount_out;
70      vblank <= next_vblank;
71      vsync_out <= vsyncon ? 0 : vsyncoff ? 1 : vsync_out;
72          // active low
73
74      blank_out <= next_vblank | (next_hblank & ~hreset);
75
76  end
77
78 endmodule


---


clk_wiz_lab3.v
1 // file: clk_wiz_lab3.v
2 //
3 // (c) Copyright 2008 - 2013 Xilinx, Inc. All rights
4 // reserved.
5 //
6 // This file contains confidential and proprietary
7 // information
8 // of Xilinx, Inc. and is protected under U.S. and
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10 // laws.
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17 // law: (1) THESE MATERIALS ARE MADE AVAILABLE "AS IS" AND
18 // WITH ALL FAULTS, AND XILINX HEREBY DISCLAIMS ALL
19 // WARRANTIES
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24 // (2) Xilinx shall not be liable (whether in contract or
25 // tort,
26 // including negligence, or under any other theory of
27 // liability) for any loss or damage of any kind or nature
28 // related to, arising under or in connection with these
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// special, incidental, or consequential loss or damage
// (including loss of data, profits, goodwill, or any type
// of
// loss or damage suffered as a result of any action brought
// by a third party) even if such damage or loss was
// reasonably foreseeable or Xilinx had been advised of the

```

```

30 // possibility of the same.
31 //
32 // CRITICAL APPLICATIONS
33 // Xilinx products are not designed or intended to be fail-
34 // safe, or for use in any application requiring fail-safe
35 // performance, such as life-support or safety devices or
36 // systems, Class III medical devices, nuclear facilities,
37 // applications related to the deployment of airbags, or any
38 // other applications that could lead to death, personal
39 // injury, or severe property or environmental damage
40 // (individually and collectively, "Critical
41 // Applications"). Customer assumes the sole risk and
42 // liability of any use of Xilinx products in Critical
43 // Applications, subject only to applicable laws and
44 // regulations governing limitations on product liability.
45 //
46 // THIS COPYRIGHT NOTICE AND DISCLAIMER MUST BE RETAINED AS
47 // PART OF THIS FILE AT ALL TIMES.
48 //
49 //

-----
```

```

50 // User entered comments
51 //
```

```

52 // None
53 //
54 //
```

```

55 // Output      Output      Phase      Duty Cycle    Pk-to-Pk
56 //          Phase
57 //          Clock      Freq (MHz)   (degrees)    (%)       Jitter (ps)
58 //          Error (ps)
```

```

59 // CLK_OUT1----65.000-----0.000-----50.0-----254.866
60 //           ----297.890
61 //
```

```

62 // Input Clock   Freq (MHz)     Input Jitter (UI)
```

```

63 // __primary-----100.000-----0.010
64
```

```

65  `timescale 1ps/1ps
66
67 module clk_wiz_lab3
68   ( // Clock in ports
69     input          clk_in1,
70   // Clock out ports
71     output         clk_out1
72   );
73
74   // Input buffering
75   //-----
76   IBUF clkin1_ibufg
77     (.O (clk_in1_clk_wiz_0),
78      .I (clk_in1));
79
80
81   // Clocking PRIMITIVE
82   //-----
83
84
85   // Instantiation of the MMCM PRIMITIVE
86   //      * Unused inputs are tied off
87   //      * Unused outputs are labeled unused
88   wire [15:0] do_unused;
89   wire       drdy_unused;
90   wire       psdone_unused;
91   wire       locked_int;
92   wire       clkfbout_clk_wiz_0;
93   wire       clkfbout_buf_clk_wiz_0;
94   wire       clkfboutb_unused;
95     wire  clkout0b_unused;
96     wire  clkout1_unused;
97     wire  clkout1b_unused;
98     wire  clkout2_unused;
99     wire  clkout2b_unused;
100    wire  clkout3_unused;
101    wire  clkout3b_unused;
102    wire  clkout4_unused;
103    wire  clkout5_unused;
104    wire  clkout6_unused;
105    wire  clkfbstopped_unused;
106    wire  clkinstopped_unused;
107
108   MMCME2_ADV
109   #( .BANDWIDTH          ("OPTIMIZED"),
110     .CLKOUT4 CASCADE      ("FALSE"),
111     .COMPENSATION        ("ZHOLD"),
112     .STARTUP_WAIT        ("FALSE"),
113     .DIVCLK_DIVIDE       (5),
114     .CLKFBOUT_MULT_F     (50.375),

```

```

115      .CLKFBOUT_PHASE      (0.000),
116      .CLKFBOUT_USE_FINE_PS ("FALSE"),
117      .CLKOUTO_DIVIDE_F    (15.500),
118      .CLKOUTO_PHASE       (0.000),
119      .CLKOUTO_DUTY_CYCLE  (0.500),
120      .CLKOUTO_USE_FINE_PS ("FALSE"),
121      .CLKIN1_PERIOD       (10.0))
122  mmcmb_adv_inst
123      // Output clocks
124  (
125      .CLKFBOUT           (clkfbout_clk_wiz_0),
126      .CLKFBOUTB          (clkfboutb_unused),
127      .CLKOUTO             (clk_out1_clk_wiz_0),
128      .CLKOUTOB            (clkout0b_unused),
129      .CLKOUT1              (clkout1_unused),
130      .CLKOUT1B             (clkout1b_unused),
131      .CLKOUT2              (clkout2_unused),
132      .CLKOUT2B             (clkout2b_unused),
133      .CLKOUT3              (clkout3_unused),
134      .CLKOUT3B             (clkout3b_unused),
135      .CLKOUT4              (clkout4_unused),
136      .CLKOUT5              (clkout5_unused),
137      .CLKOUT6              (clkout6_unused),
138      // Input clock control
139      .CLKFBIN              (clkfbout_buf_clk_wiz_0),
140      .CLKIN1                (clk_in1_clk_wiz_0),
141      .CLKIN2                (1'b0),
142      // Tied to always select the primary input clock
143      .CLKINSEL              (1'b1),
144      // Ports for dynamic reconfiguration
145      .DADDR                 (7'h0),
146      .DCLK                  (1'b0),
147      .DEN                   (1'b0),
148      .DI                     (16'h0),
149      .DO                     (do_unused),
150      .DRDY                  (drdy_unused),
151      .DWE                   (1'b0),
152      // Ports for dynamic phase shift
153      .PSCLK                 (1'b0),
154      .PSEN                   (1'b0),
155      .PSINCDEC              (1'b0),
156      .PSDONE                 (psdone_unused),
157      // Other control and status signals
158      .LOCKED                 (locked_int),
159      .CLKINSTOPPED          (clkinstopped_unused),
160      .CLKFBSTOPPED          (clkfbstopped_unused),
161      .PWRDWN                 (1'b0),
162      .RST                     (1'b0));
163
164

```

```

165      // Output buffering
166      //-----
167
168      BUFG clkf_buf
169      (.O (clkfbout_buf_clk_wiz_0),
170       .I (clkfbout_clk_wiz_0));
171
172
173
174      BUFG clkout1_buf
175      (.O (clk_out1),
176       .I (clk_out1_clk_wiz_0));
177
178
179
180
181
182 endmodule


---


display_8hex.sv


---


1
2 //////////////////////////////////////////////////////////////////
3 // Engineer:    g.p.hom
4 //
5 // Create Date: 18:18:59 04/21/2013
6 // Module Name: display_8hex
7 // Description: Display 8 hex numbers on 7 segment display
8 //
9 //
////////////////////////////////////////////////////////////////

10
11 module display_8hex(
12     input  clk_in,           // system clock
13     input [31:0] data_in,    // 8 hex numbers, msb
14             first,
15     output reg [6:0] seg_out, // seven segment display
16             output
17     output reg [7:0] strobe_out // digit strobe
18 );
19
20     localparam bits = 13;
21
22     reg [bits:0] counter = 0; // clear on power up
23
24     wire [6:0] segments[15:0]; // 16 7 bit memorys
25     assign segments[0] = 7'b100_0000; // inverted logic
26     assign segments[1] = 7'b111_1001; // gfedcba

```

```

25      assign segments[2] = 7'b010_0100;
26      assign segments[3] = 7'b011_0000;
27      assign segments[4] = 7'b001_1001;
28      assign segments[5] = 7'b001_0010;
29      assign segments[6] = 7'b000_0010;
30      assign segments[7] = 7'b111_1000;
31      assign segments[8] = 7'b000_0000;
32      assign segments[9] = 7'b001_1000;
33      assign segments[10] = 7'b000_1000;
34      assign segments[11] = 7'b000_0011;
35      assign segments[12] = 7'b010_0111;
36      assign segments[13] = 7'b010_0001;
37      assign segments[14] = 7'b000_0110;
38      assign segments[15] = 7'b000_1110;
39
40      always_ff @(posedge clk_in) begin
41          // Here I am using a counter and select 3 bits which
42          // provides
43          // a reasonable refresh rate starting the left most
44          // digit
45          // and moving left.
46          counter <= counter + 1;
47          case (counter[bits:bits-2])
48              3'b000: begin // use the MSB 4 bits
49                  seg_out <= segments[data_in[31:28]];
50                  strobe_out <= 8'b0111_1111 ;
51              end
52
53              3'b001: begin
54                  seg_out <= segments[data_in[27:24]];
55                  strobe_out <= 8'b1011_1111 ;
56              end
57
58              3'b010: begin
59                  seg_out <= segments[data_in[23:20]];
60                  strobe_out <= 8'b1101_1111 ;
61              end
62
63              3'b011: begin
64                  seg_out <= segments[data_in[19:16]];
65                  strobe_out <= 8'b1110_1111;
66              end
67
68              3'b100: begin
69                  seg_out <= segments[data_in[15:12]];
70                  strobe_out <= 8'b1111_0111;
71              end
72
73              3'b101: begin
74                  seg_out <= segments[data_in[11:8]];
75                  strobe_out <= 8'b1111_1011;
76              end

```

```

73
74      3'b110: begin
75          seg_out <= segments[data_in[7:4]];
76          strobe_out <= 8'b1111_1101;
77      end
78      3'b111: begin
79          seg_out <= segments[data_in[3:0]];
80          strobe_out <= 8'b1111_1110;
81      end
82
83  endcase
84 end
85
86 endmodule


---


initialize.sv
1  `timescale 1ns / 1ps
2
3 //given the camera pixel, outputs everything to display
4 module initialize(
5     input clk_65mhz,
6     input reset,
7     input [10:0] hcount,
8     input [9:0] vcount,
9     input vsync,
10    input [3:0] directions, //up,down,left,right
11    input confirm_in,
12    input activate_in,
13    input sw2, //whether to make the size twice
14    input [11:0] cam,
15    input [8:0] cur_pos_x,
16    input [8:0] cur_pos_y,
17    input [6:0] cur_rad,
18    input signed [8:0] speed1,speed2,
19    output logic [11:0] pixel_out,
20    output logic [11:0] goal_pixel,
21    output logic [6:0] goal_rad,
22    output logic track,
23    output logic move,
24    //for debug
25    output logic [2:0] state,
26    output logic [10:0] cursor_x,
27    output logic [9:0] cursor_y,
28    output logic up,down,left,right
29 );
30
31 logic [8:0] height;
32 logic [9:0] width;
33
34 assign height = sw2?9'd480:9'd240;

```

```

35     assign width = sw2?10'd640:10'd320;
36
37
38 //generate the blobs
39 logic [11:0] box,box_confirmed,cursor,pad,speed_bar,
    selected_pixel,selected_buff,goal_pad;
40 //logic [10:0] cursor_x;
41 //logic [9:0] cursor_y;
42
43 box box_gen(.x_in({2'b00,cur_pos_x}), .y_in({1'b0,
    cur_pos_y}), .hcount_in(hcount), .vcount_in(vcount), .
    radius_in(cur_rad), .pixel_out(box));
44 box #(.COLOR(12'hf00)) confirmed_box_gen (.x_in({2'b00,
    cur_pos_x}), .y_in({1'b0,cur_pos_y}), .hcount_in(hcount
    ), .vcount_in(vcount), .radius_in(cur_rad), .pixel_out(
    box_confirmed));
45 cursor cursor_gen(.x_in(cursor_x), .y_in(cursor_y), .
    hcount_in(hcount), .vcount_in(vcount), .sw2(sw2), .
    pixel_out(cursor));
46 colorpad colorpad_gen(.pixel_in(selected_buff), .hcount_in
    (hcount), .vcount_in(vcount), .pixel_out(pad));
47 colorpad goal_colorpad_gen(.pixel_in(goal_pixel), .
    hcount_in(hcount), .vcount_in(vcount), .pixel_out(
    goal_pad));
48 speed_bar speed_bar_gen(.speed1(speed1), .speed2(speed2),
    .hcount_in(hcount), .vcount_in(vcount), .pixel_out(
    speed_bar));
49
50 ////////////////////////////////cursor control
51 ///////////////////////////////
52
53 parameter CURSORSPEED = 3;
54 parameter SAMPLESIZE = 1; // (0 -> 1, 1 -> 4, 2 -> 16)
55
56 // logic up,down,left,right;
57 logic [7:0] sum_r,sum_g,sum_b,sum_r_d,sum_g_d,sum_b_d;
58 logic [3:0] shifted_r,shifted_g,shifted_b;
59
60 assign shifted_r = sum_r >> 4;
61 assign shifted_g = sum_g >> 4;
62 assign shifted_b = sum_b >> 4;
63
64 //single sample
65 //assign selected_pixel = (vcount == cursor_y && hcount ==
66 //    cursor_x)? cam:selected_pixel;
67
68 //assign selected_pixel = {shifted_r,shifted_g,shifted_b};
69 logic confirm,confirm_serial,old_confirmed,activate;
70 assign confirm = confirm_serial & ~old_confirmed; //pulse

```

```

69
70     debounce db1(.reset_in(reset),.clock_in(clk_65mhz),.
71                 noisy_in(directions[3]),.clean_out(up));
72     debounce db2(.reset_in(reset),.clock_in(clk_65mhz),.
73                 noisy_in(directions[2]),.clean_out(down));
74     debounce db3(.reset_in(reset),.clock_in(clk_65mhz),.
75                 noisy_in(directions[1]),.clean_out(left));
76     debounce db4(.reset_in(reset),.clock_in(clk_65mhz),.
77                 noisy_in(directions[0]),.clean_out(right));
78     debounce db5(.reset_in(reset),.clock_in(clk_65mhz),.
79                 noisy_in(confirm_in),.clean_out(confirm_serial));
80     debounce db6(.reset_in(reset),.clock_in(clk_65mhz),.
81                 noisy_in(activate_in),.clean_out(activate));
82
83     always_ff @(posedge vsync) begin
84         if(reset) begin
85             cursor_x <= 11'h00f;
86             cursor_y <= 10'h00f;
87
88             //selected_buff <= 12'hff0;
89         end else begin
90             if (up) begin
91                 if(cursor_y < CURSORSPEED) cursor_y <= 0;
92                 else cursor_y <= cursor_y - CURSORSPEED;
93
94             end
95
96             if (down) begin
97                 if (cursor_y > height - CURSORSPEED) cursor_y <=
98                     height;
99                 else cursor_y <= cursor_y + CURSORSPEED;
100            end
101
102            if (left) begin
103                if(cursor_x < CURSORSPEED) cursor_x <= 0;
104                else cursor_x <= cursor_x - CURSORSPEED;
105            end
106        end
107
108 //    always_ff @(posedge clk_65mhz) begin
109 //        //update pixel selected by cursor (average 4 or 16bits
110 //        around)

```

```

110 //      if ((vcount >= cursor_y - SAMPLESIZE && vcount <
111 //          cursor_y) && (hcount >= cursor_x - SAMPLESIZE && hcount <
112 //          cursor_x + SAMPLESIZE)) begin
113 //          sum_r <= sum_r + cam[11:8];
114 //          sum_g <= sum_g + cam[7:4];
115 //          sum_b <= sum_b + cam[3:0];
116 //      end
117 //      if(vcount == 10'd550 && hcount ==11'd750) begin
118 //          sum_r <= 0;
119 //          sum_g <= 0;
120 //          sum_b <= 0;
121 //          selected_buff <= selected_buff + 1;
122 //          selected_buff <= 12'hf00;
123 //      end
124 //end //end always_ff
125 ////////////////////////////////////////////////end cursor
126 control/////////////////////////////////
127 //////////////////////////////////////////////main FSM
128 parameter INITIALIZE = 0;
129 parameter SELECTED = 1;
130 parameter CONFIRMED = 2;
131 parameter MOVE = 3;
132 parameter PAUSE = 4;
133
134 //logic [1:0] state;
135 logic [2:0] old_state;
136 logic old_activate;
137 logic activated;
138 logic selected;
139 logic confirmed;
140
141 assign activated = ~old_activate & activate;           //if
142 //switched to activated
143 assign selected = (state==SELECTED && old_state==INITIALIZE)
144 ;;
145 assign confirmed = (state==CONFIRMED && old_state==SELECTED)
146 ;;
147
148 always_ff @(posedge clk_65mhz) begin
149     if(reset) begin
150         //initialize
151         old_state <= 0;
152         old_activate <= 0;
153         state <= INITIALIZE;
154         goal_rad <= 0;
155         goal_pixel <= 0;

```

```

153     pixel_out <= 0;
154     old_confirmed <= 0;
155     selected_buff <= 12'h000;
156     sum_r <= 0;
157     sum_g <= 0;
158     sum_b <= 0;
159   end else begin
160     //pad
161     if(vcount == cursor_y && hcount == cursor_x)
162       selected_buff <= cam;
163     if ((vcount >= cursor_y - SAMPLESIZE && vcount <
164         cursor_y) && (hcount >= cursor_x - SAMPLESIZE &&
165         hcount < cursor_x + SAMPLESIZE)) begin
166       sum_r <= sum_r + cam[11:8];
167       sum_g <= sum_g + cam[7:4];
168       sum_b <= sum_b + cam[3:0];
169     end
170     if(vcount == 10'd550 && hcount == 11'd750) begin
171       sum_r <= 0;
172       sum_g <= 0;
173       sum_b <= 0;
174     //      selected_buff <= {sum_r[5:2],sum_g[5:2],sum_b
175     [5:2]};
176     //      selected_buff <= 12'hf00;
177   end
178
179   old_state <= state;
180   old_activate <= activate;
181   old_confirmed <= confirm_serial;
182   //switch to initialize every time activated
183   if(activated) state <= INITIALIZE;
184   //get the goal pixel
185   if(selected) goal_pixel <= selected_buff;
186   //get the goal radius
187   if(confirmed) goal_rad <= cur_rad;
188
189   case(state)
190     INITIALIZE: begin
191       track <= 0;
192       move <= 0;
193       if(confirm) state <= SELECTED;
194       pixel_out <= &cursor?cursor:cam+pad;
195     end
196     SELECTED: begin
197       track <= 1;
198       move <= 0;
199       if(up | down | left | right) state <= INITIALIZE
200       ;
201       if(confirm) state <= CONFIRMED;
202       pixel_out <= (&cursor | &box)?cursor+box:cam +

```

```

        goal_pad;
198
199      end
200      CONFIRMED: begin
201          track <= 1;
202          move <= 0;
203          if(~activate) state <= MOVE;
204          pixel_out <= &box?box_confirmed:cam+speed_bar+
205              goal_pad;
206          end
207          MOVE: begin
208              track <= 1;
209              move <= 1;
210              pixel_out <= &box?box_confirmed:cam+goal_pad+
211                  speed_bar;
212              if(confirm) state <= PAUSE;
213              end
214              PAUSE: begin
215                  track <= 0;
216                  move <= 0;
217                  pixel_out <= &box?box_confirmed:cam+goal_pad+
218                      speed_bar;
219                  if(confirm) state <= MOVE;
220                  end
221          endcase
222      end
223  endmodule

```

control.sv

```

1  `timescale 1ns / 1ps
2
3
4  module control(
5      input clk_in,
6      input rst_in,
7      input ready_in,
8      input [8:0] cur_pos_x,
9      input [8:0] cur_pos_y,
10     input [6:0] cur_rad,
11     input [6:0] goal_rad,
12     input [15:0] params,
13     output logic signed [8:0] speed,
14     output logic signed [8:0] turn
15 );
16
17 //camera size
18 parameter HEIGHT = 240;
19 parameter WIDTH = 320;

```

```

20
21 //modes
22 parameter FORWARD = 0;
23 parameter DIRECT = 1;
24 parameter GOALKEEP = 3;
25 parameter CHASE = 2;
26
27 //assign params
28 logic signed [4:0] Ksp;
29 logic signed [3:0] Ksd;
30 logic signed [4:0] Ktp;
31 logic signed [3:0] Ktd;
32 logic [1:0] mode;
33
34 assign {Ksp[3:0],Ksd[2:0],Ktp[3:0],Ktd[2:0],mode} = params;
35
36 assign Ksp[4] = 0;
37 assign Ksd[3] = 0;
38 assign Ktp[4] = 0;
39 assign Ktd[3] = 0;
40
41 //desired x,r
42 logic [8:0] x_d;
43 logic [6:0] r_d;
44 assign x_d = WIDTH >> 1;
45 assign r_d = goal_rad;
46
47 //current x,rad,dx,dr
48 logic [8:0] x;
49 logic [6:0] r;
50 logic [8:0] dx;
51 logic [6:0] dr;
52
53 //previous x,rad,dx,dr
54 logic [8:0] pre_x;
55 logic [6:0] pre_r;
56 logic [8:0] pre_dx;
57 logic [6:0] pre_dr;
58
59
60 //errors
61 logic signed [8:0] e_x;
62 logic signed [8:0] e_r;
63 logic signed [8:0] e_dx;
64 logic signed [8:0] e_dr;
65
66 assign e_x = x_d - x; //abs less than 240
67 assign e_r = r_d - r;
68
69

```

```

70  //raw speed,turn
71  logic signed [16:0] raw_speed;
72  logic signed [16:0] raw_turn;
73
74
75  //threshold the output
76  logic [7:0] pass1;
77  logic [7:0] pass2;
78
79  threshold_by_abs threshold_speed(.signed_in(raw_speed), .
    threshold(16'h00ff), .signed_out({speed[8],pass1,speed[7:
    0]}));
80  threshold_by_abs threshold_turn(.signed_in(raw_turn), .
    threshold(16'h00ff), .signed_out({turn[8],pass2,turn[7:0]
})) );
81
82
83
84  always_comb begin
85      case(mode)
86          GOALKEEP:begin
87              raw_speed = (Ksp * e_x) + (Ksd * e_dx);
88              raw_turn = 0;
89
90          end
91          CHASE: begin
92              raw_speed = (Ksp * e_r) + (Ksd * e_dr);
93              raw_turn = (Ktp * e_x) + (Ktd * e_dx);
94          end
95          DIRECT: begin
96              raw_speed = {params[15],8'd0,params[14:8]
97                          ,1'b0};
98              raw_turn = {params[7],8'd0,params[6:0],1'
99                          b0};
100         end
101     default:begin
102             raw_speed = 0;
103             raw_turn = 0;
104         end
105     endcase
106  end
107
108  always_ff @(posedge clk_in) begin
109      if(rst_in) begin
110          //initialize
111          x <= 0;
112          r <= 0;
113          dx <= 0;
114          dr <= 0;
115          pre_x <= 0;

```

```

114     pre_r <= 0;
115     pre_dx <= 0;
116     pre_dr <= 0;
117   end
118
119   else begin
120     if(ready_in) begin
121       x <= cur_pos_x;
122       r <= cur_rad;
123       e_dx <= x - cur_pos_x;
124       e_dr <= r - cur_rad;
125     end
126   end
127 end
128 endmodule
129
130
131
132 module threshold_by_abs(
133   input signed [16:0] signed_in,
134   input [15:0] threshold,
135   output signed [16:0] signed_out
136 );
137
138 logic sign;
139 logic [15:0] abs;
140
141 assign sign = signed_in[16];
142 assign signed_out[16] = sign;
143
144 assign abs = sign?~signed_in[15:0] + 16'h0001:signed_in[15:0
145   ];
146 assign signed_out[15:0] = (abs <= threshold)? signed_in[15:0
147   ]:(sign?~threshold+16'h0001:threshold);
148 endmodule


---


motor_out.sv
1 'timescale 1ns / 1ps
2
3 module motor_out(input clk_in,
4                   input rst_in,
5                   input [7:0] offset, //minimum speed needed
6                               to drive the car
7                   input signed [8:0] speed_in,
8                   input signed [8:0] turn_in,
9                   output logic [5:0] motor_out, //en1,ina1,
10                      inb1,ina2,inb2,en2
11                   );

```

```

12
13 logic signed [9:0] raw_motor1;
14 logic signed [9:0] raw_motor2;
15 logic [8:0] expanded_1;
16 logic [8:0] expanded_2;
17 logic [7:0] speed_1_offset; //without offset
18 logic [7:0] speed_2_offset; //without offset
19
20 logic forward_1;
21 logic forward_2;
22
23 assign raw_motor1 = speed_in - (turn_in >>> 1);
24 assign raw_motor2 = speed_in + (turn_in >>> 1);
25
26 assign forward_1 = ~raw_motor1[9];
27 assign forward_2 = ~raw_motor2[9];
28
29 assign expanded_1 = forward_1?raw_motor1[8:0]:~raw_motor1[8:
    0] + 9'h001;
30 assign expanded_2 = forward_2?raw_motor2[8:0]:~raw_motor2[8:
    0] + 9'h001;
31
32 assign speed_1_offset = expanded_1[8]?8'hff:expanded_1[7:0];
33 assign speed_2_offset = expanded_2[8]?8'hff:expanded_2[7:0];
34
35 assign speed_1 = (speed_1_offset>8'hff-offset)?8'hff:
    speed_1_offset+offset;
36 assign speed_2 = (speed_2_offset>8'hff-offset)?8'hff:
    speed_2_offset+offset;
37
38 pwm en1(.clk_in(clk_in), .rst_in(rst_in), .level_in(speed_1)
    , .pwm_out(motor_out[5]));
39 pwm en2(.clk_in(clk_in), .rst_in(rst_in), .level_in(speed_2)
    , .pwm_out(motor_out[0]));
40
41 assign motor_out[4:1] = {forward_1,~forward_1,forward_2,~
    forward_2};
42
43
44
45 endmodule
46
47
48 module pwm (input clk_in, input rst_in, input [7:0] level_in
    , output logic pwm_out);
49     logic [7:0] count;
50     assign pwm_out = count<level_in;
51     always_ff @(posedge clk_in)begin
52         if (rst_in)begin
53             count <= 8'b0;

```

```

54         end else begin
55             count <= count+8'b1;
56         end
57     end
58 endmodule


---


color_class.sv
1  `timescale 1ns / 1ps
2  /*
3   // Company:
4   // Engineer:
5   //
6   // Create Date: 12/09/2019 02:46:49 PM
7   // Design Name:
8   // Module Name: color_class
9   // Project Name:
10  // Target Devices:
11  // Tool Versions:
12  // Description:
13  //
14  // Dependencies:
15  //
16  // Revision:
17  // Revision 0.01 - File Created
18  // Additional Comments:
19  //
20  //
21  /*
22
23 module color_class(
24     input [7:0] h,
25     input [7:0] s,
26     input [7:0] v,
27     output reg [2:0] cls );
28 always_comb begin
29     if ((h<=8'd3) &&(s>8'd50)&&(v>8'd50)) cls=3'b001;
30     else if ((h>8'd3)&&(h<8'd10)&&(s>8'd100)&&(v>8'd100))
31         cls=3'b100;
32     else begin
33         if ((h<=8'd32)&& (h>8'd20) &&(s>8'd100)&&( v>8'd100)
34             ) cls=3'b010; // yellow
35     else begin
36         if ((h<=8'd32) &&(s>8'd100)&&( v>8'd100)) cls=3'b011
37             ;
38         else cls=3'b111;
39     end

```

```
37      end
38  end
39
40 endmodule
```