6.111 Final Project Checklist
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Goal	Description	Scheduled Completion Date	Actual Completion Date
Base DPU	DPU implementation is correct. Starting state hardcoded. Can reset to initial state.	18 Nov	
Optimized DPU	DPU implementation is correct and minimal. Load starting states without recompiling.	25 Nov	
Large N DPU	More particles than DPUs. Requires major architectural change.	2 Dec	
2D display	Fixed 2D display of simulation from top, bottom, side, and isometric. Switch between displays with buttons on Nexys. Use VGA display strategy from Lab 2.	18 Nov	
3D display	Display of simulation in 3D from arbitrary angle. Change angle using directional pad on Nexys. Zoom in and out with center button.	25 Nov	
3D interface	Display of simulation in 3D from arbitrary angle. Change angle and zoom by rotating, moving IMU module. Connect IMU module to Nexys wirelessly using BLE (BLE module with PSoC connected to Nexys).	2 Dec	
Integration & Testing	Communication protocol is consistent between DPUs and the Graphics module. FPGA simulation results match reference.	9 Dec	
Demo & Checkoff	Setup system in lab. Run comparison with C implementation.	13 Dec	

Red — Minimum Viable Product
Yellow — Complete and Functioning Product
Green — Additionally Featured Product