
DDR Whack-a-mole!

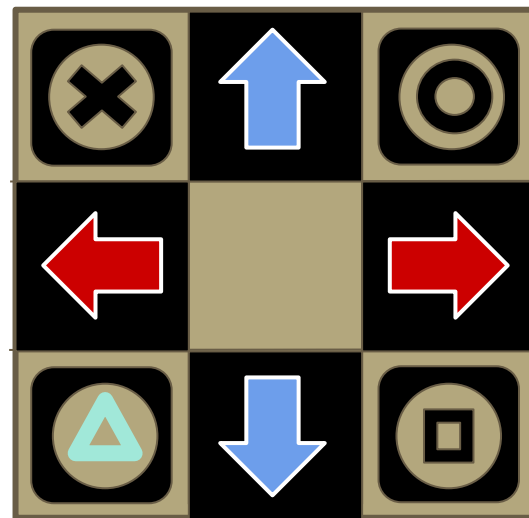
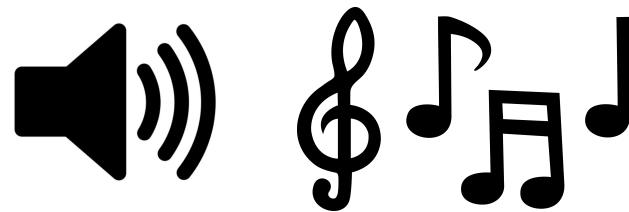
Ara Adhikari, Victoria Ouyang, Davis Tran

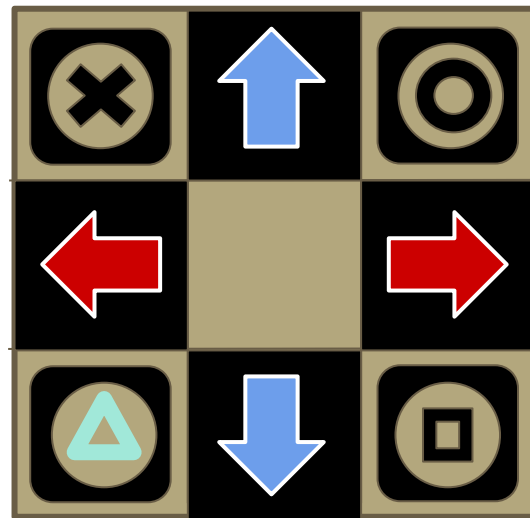
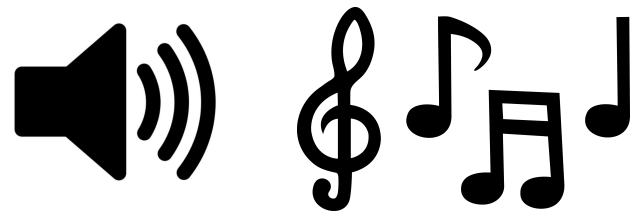
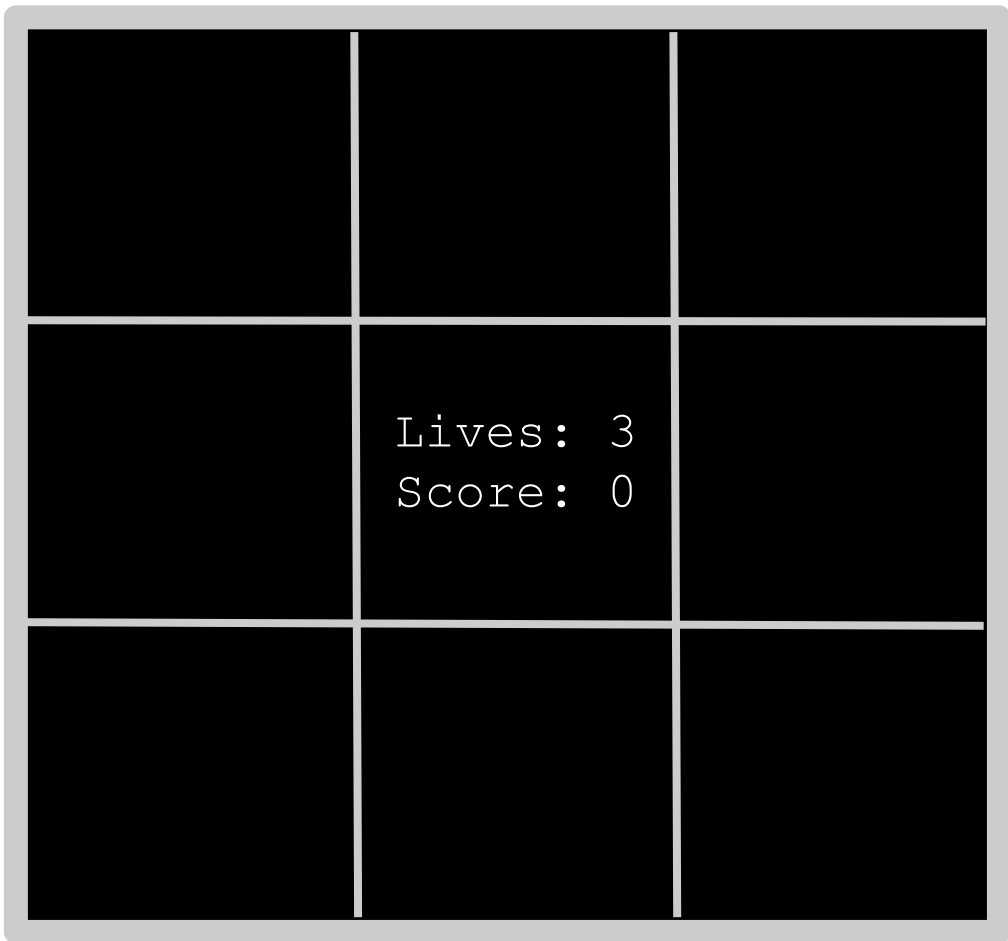


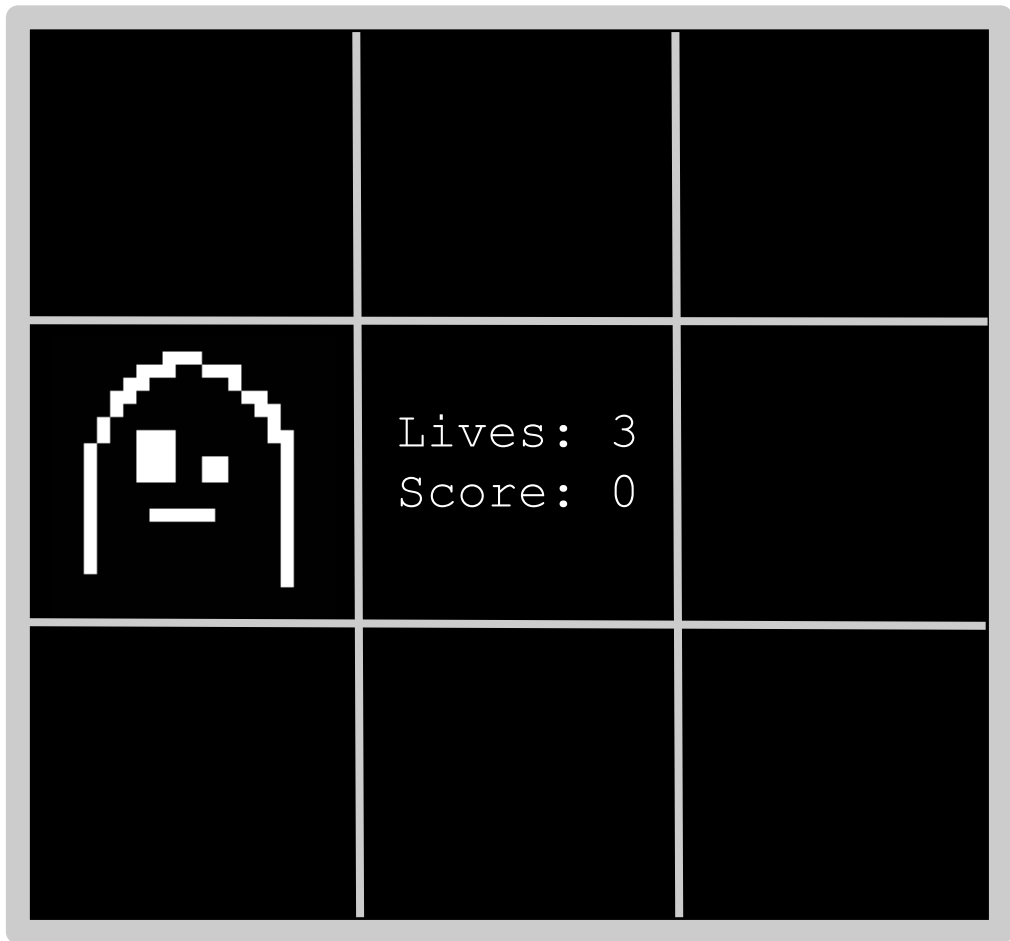
Game Demo

DDR
Whack-a-Mole!

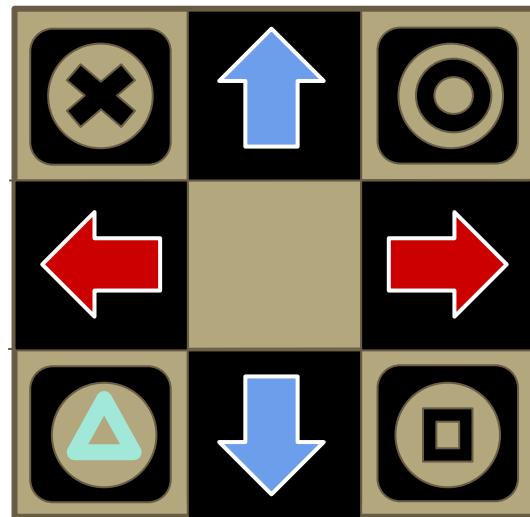
Press  to play

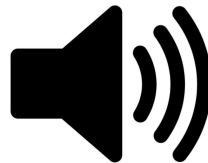
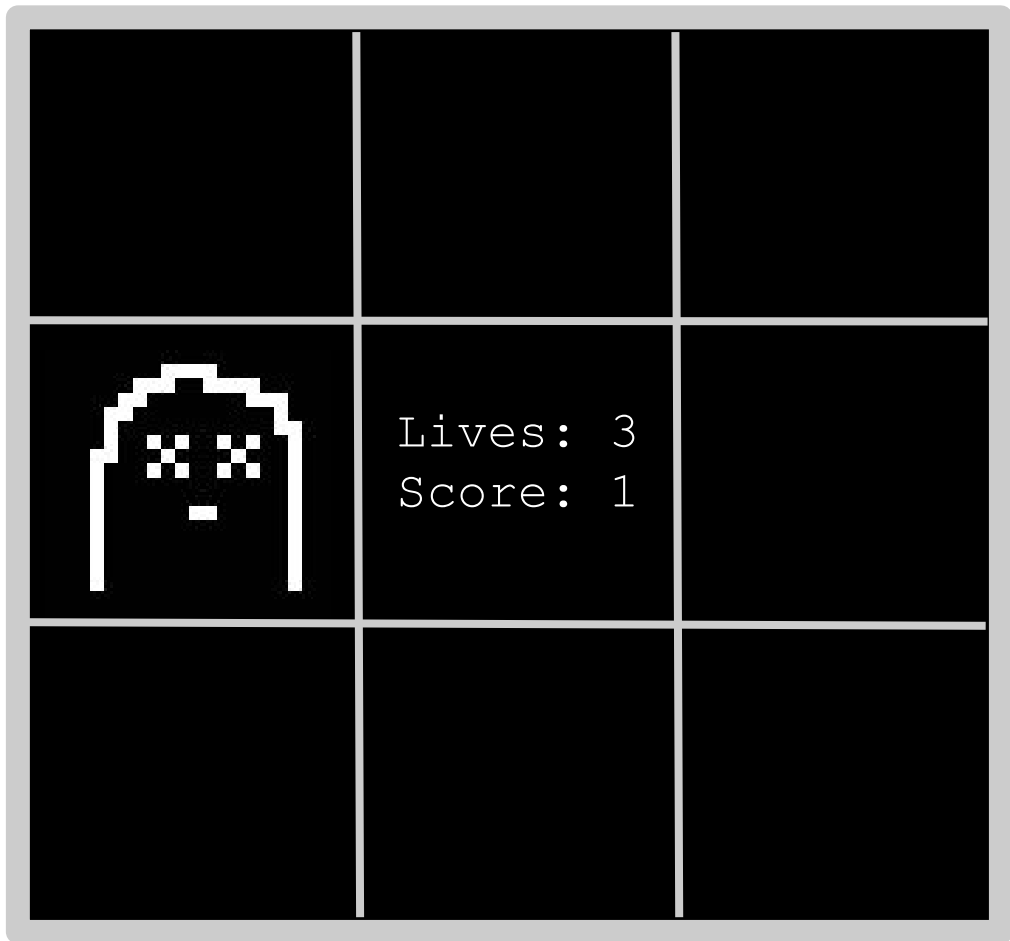




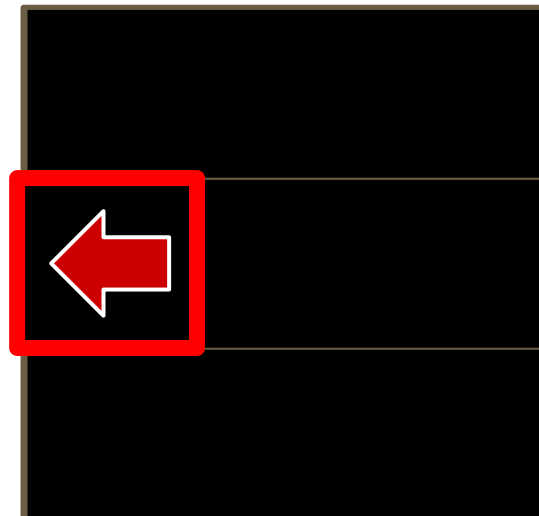


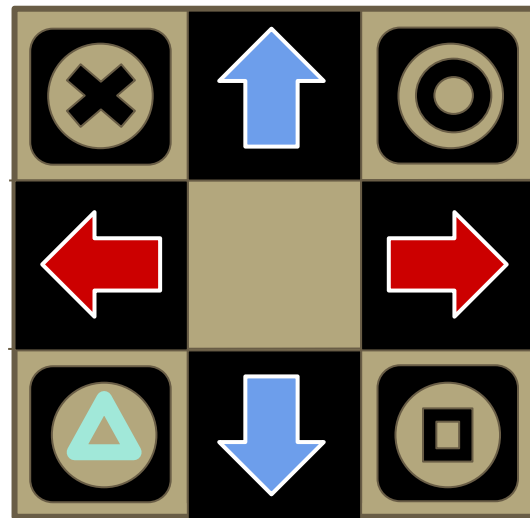
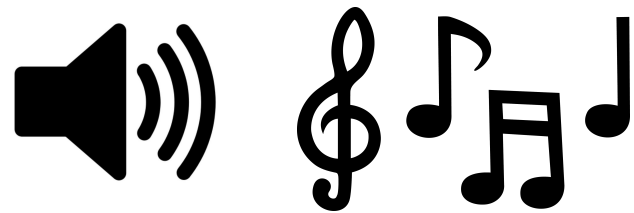
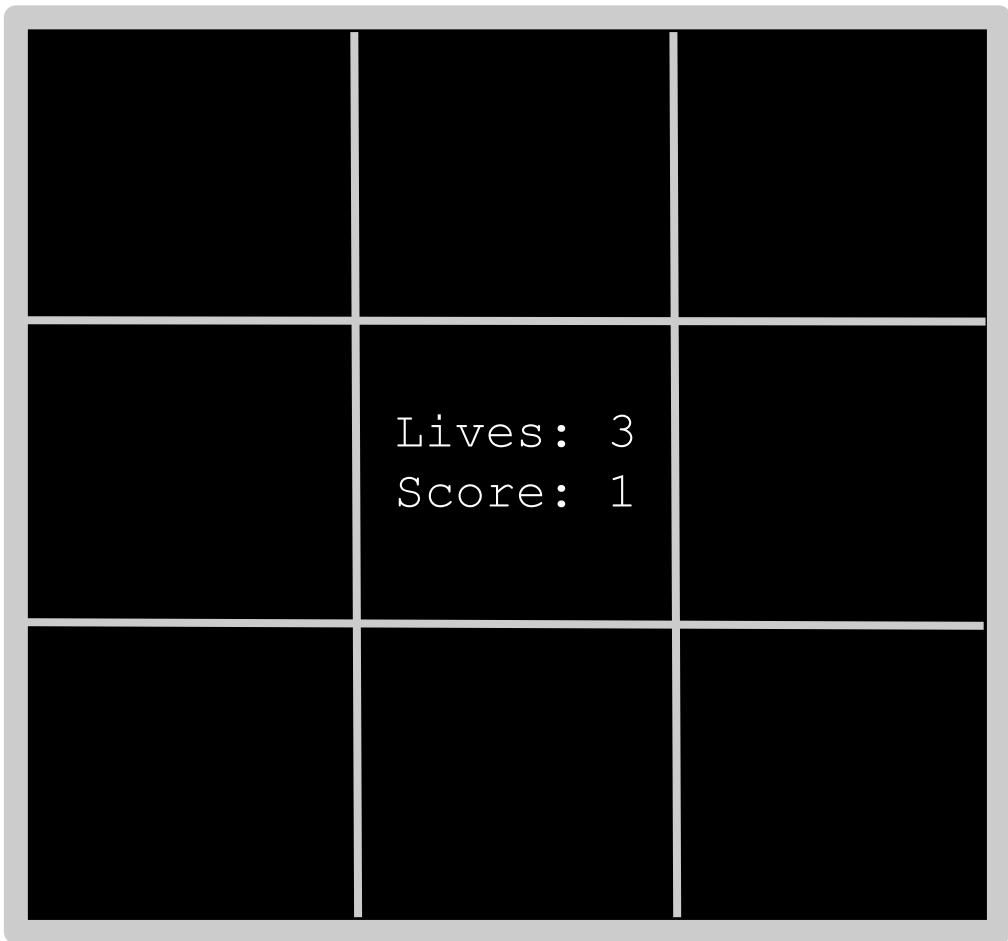
Mole Sound

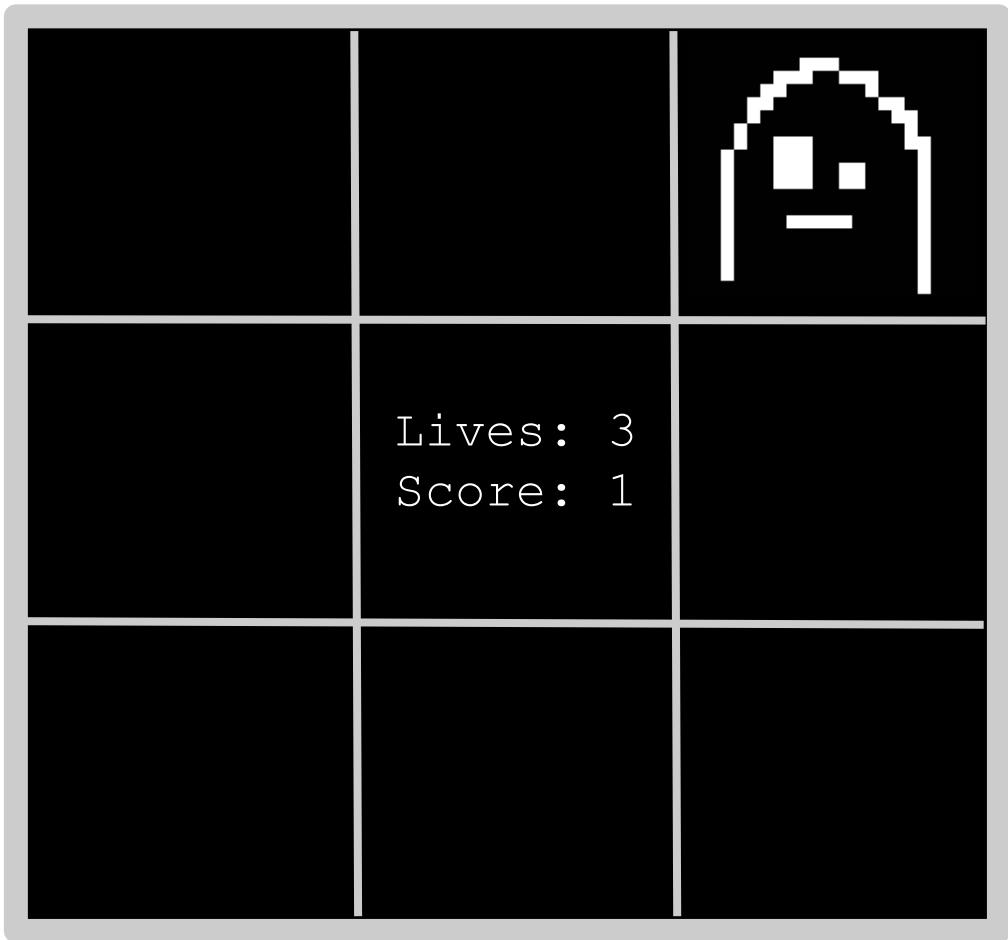




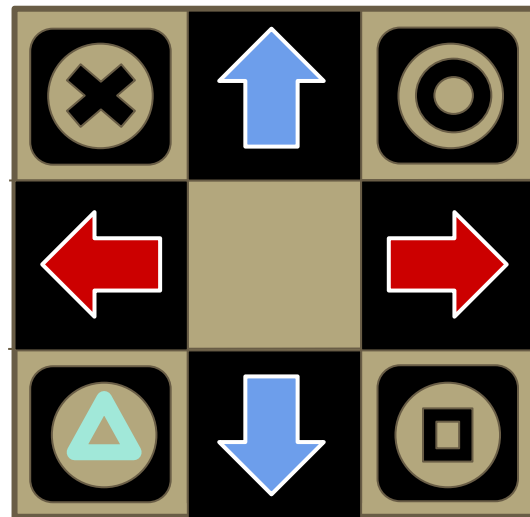
*Dead Mole
Sound*

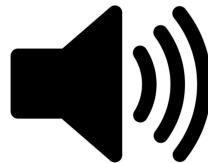
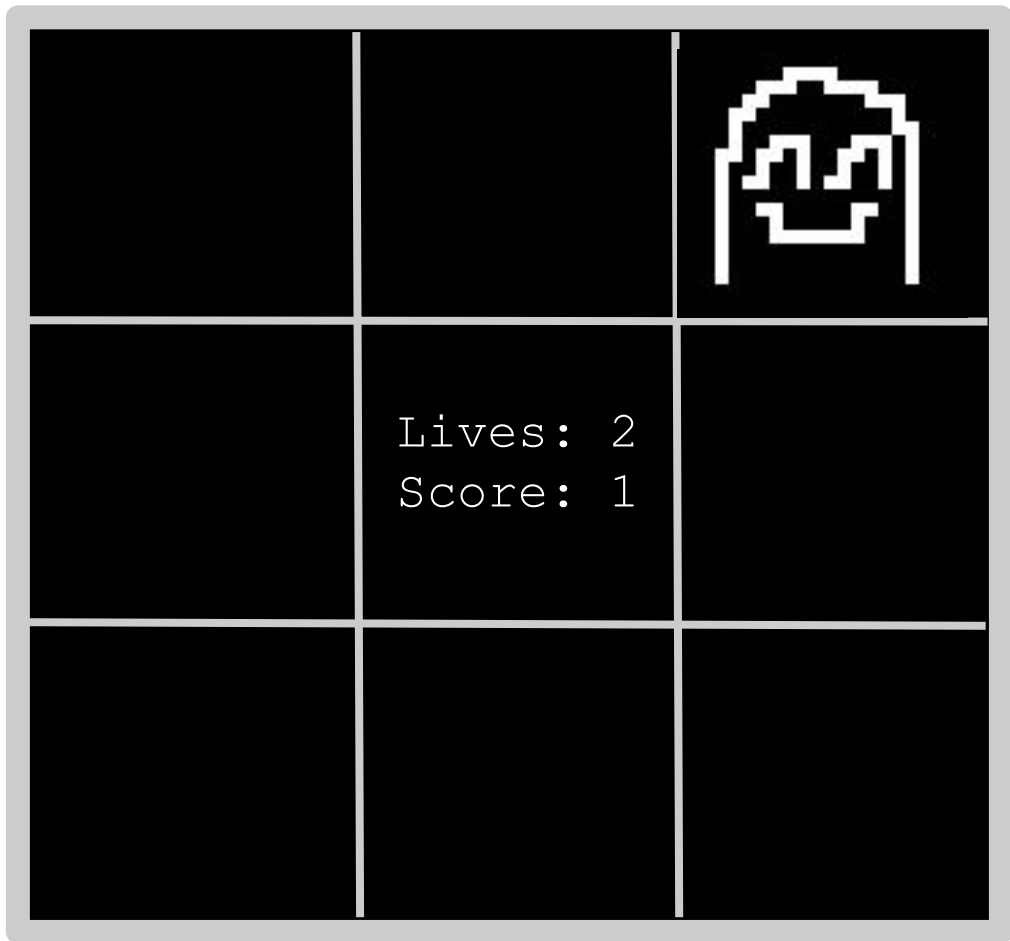




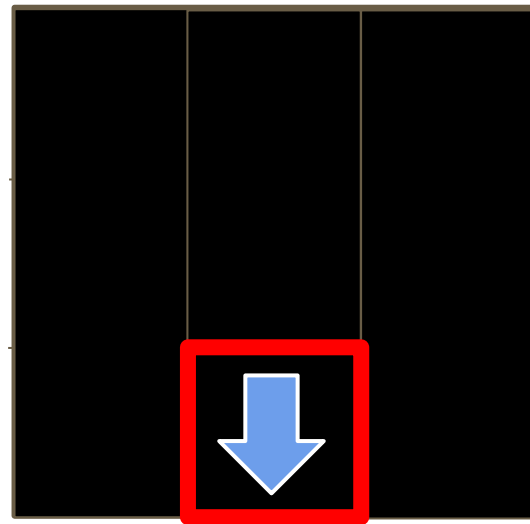


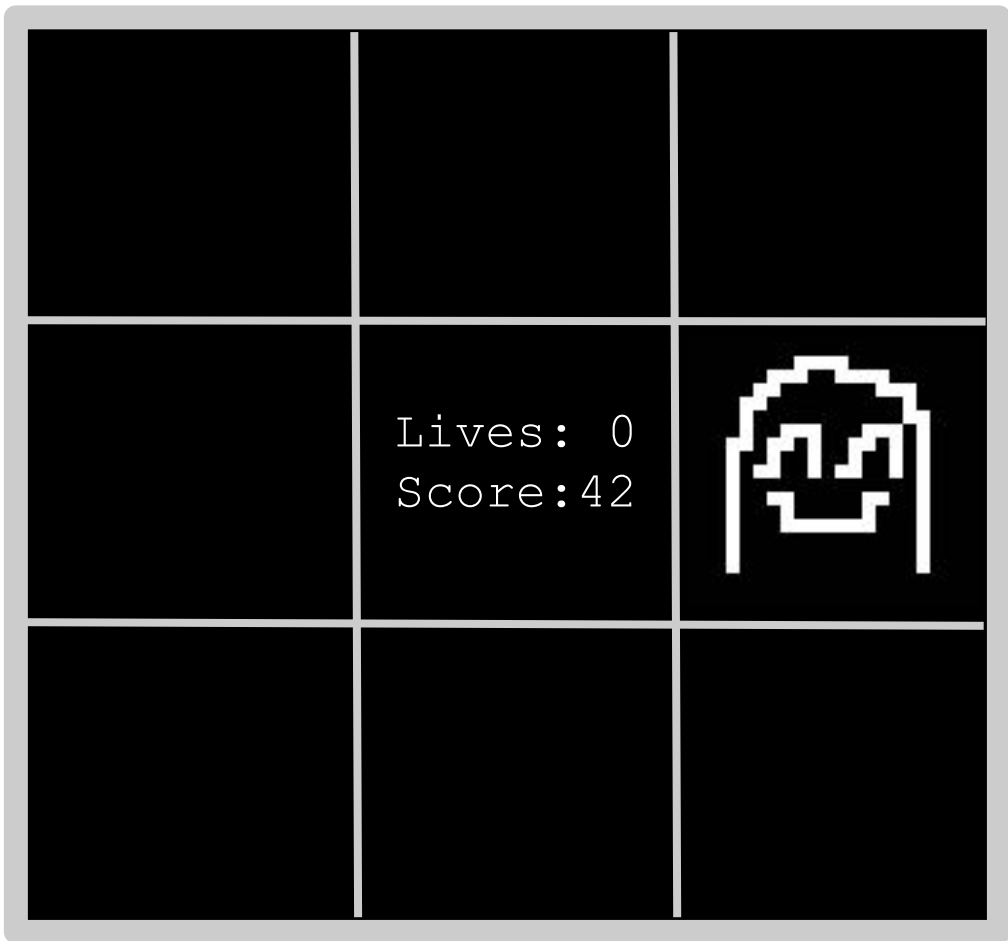
Mole Sound



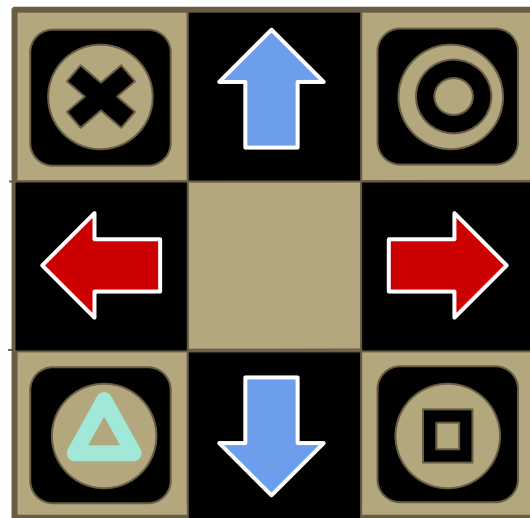


Mole Cackle





Mole Cackle



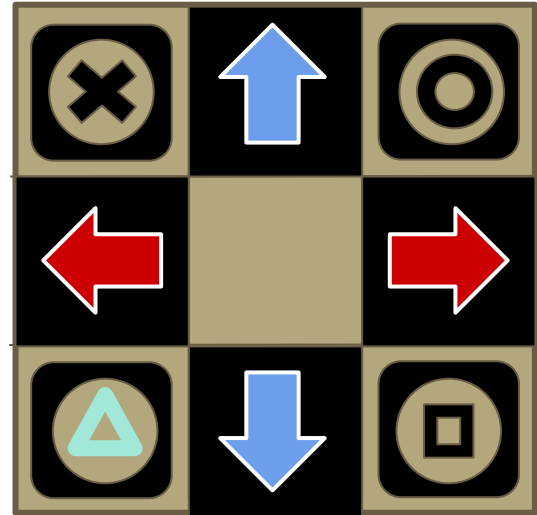
Game Over

Score: 42

Press  to play



*Game Over
Noise*



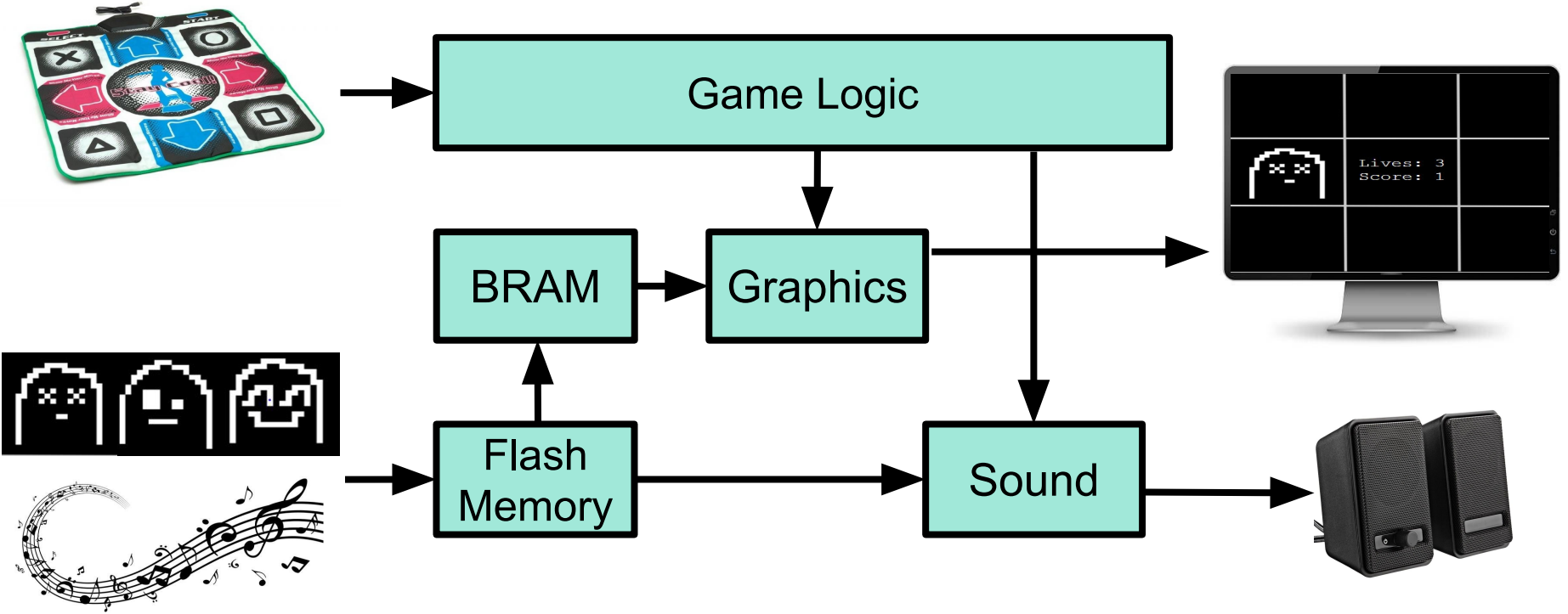
Why Do We Want To Do This?

Fun (game, dance-related)

Interactive

Expandable

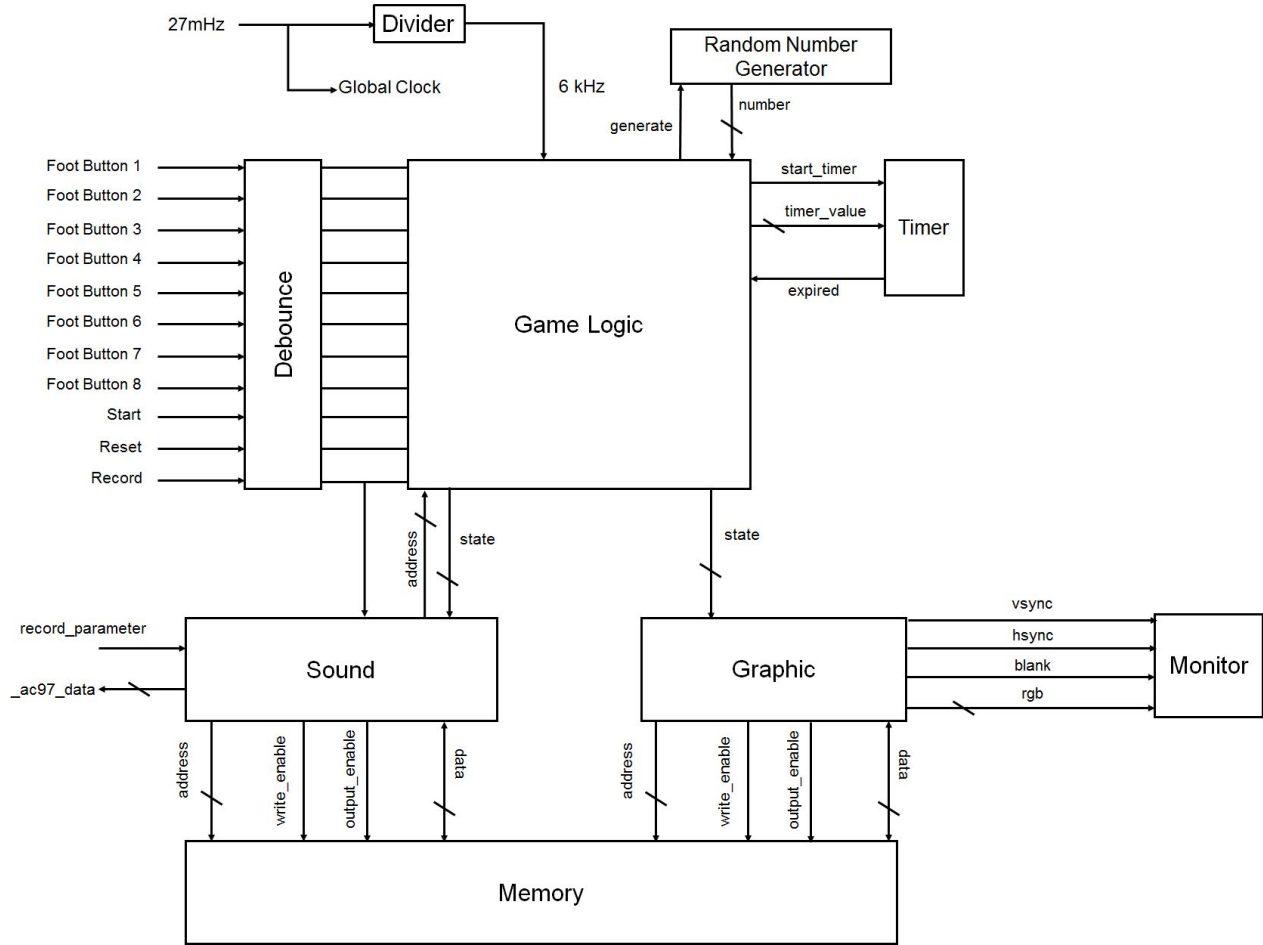
Overall Design



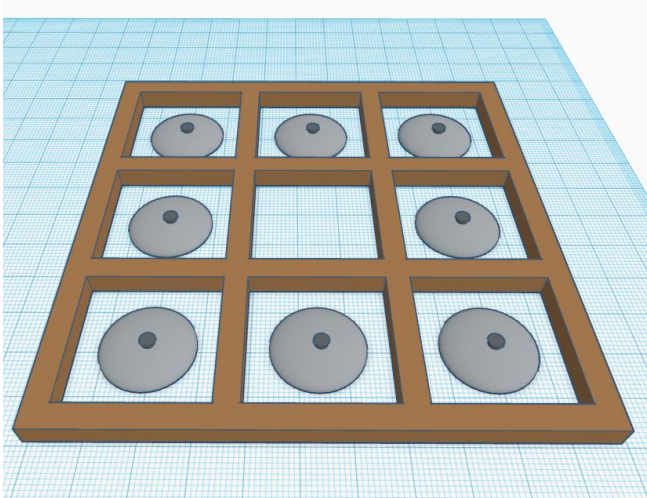
Block Diagram



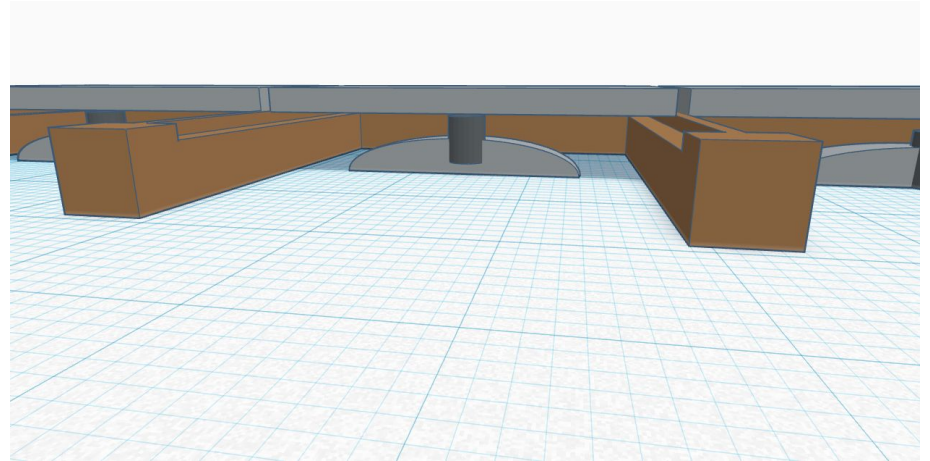
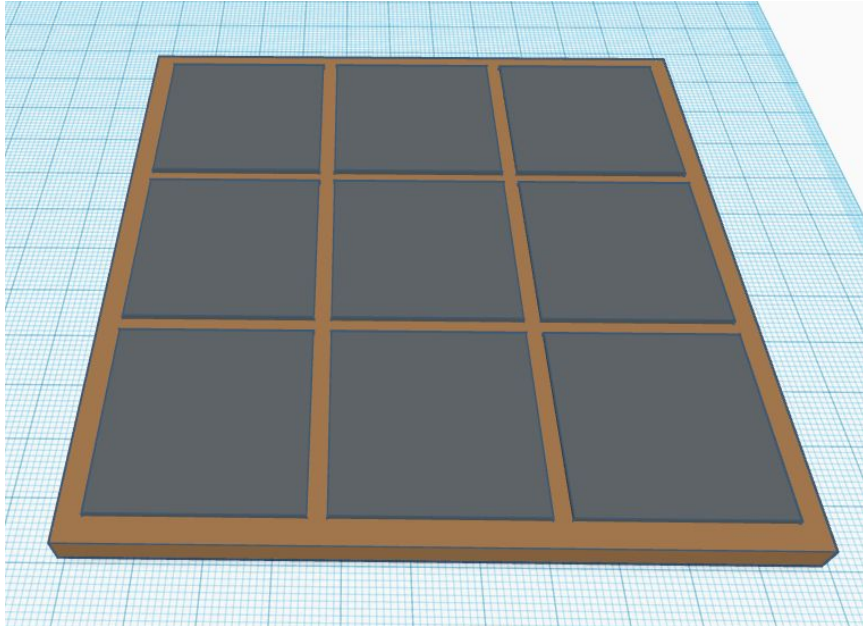
6.111 Labkit



Customized Board



Customized Board



Game Logic Module

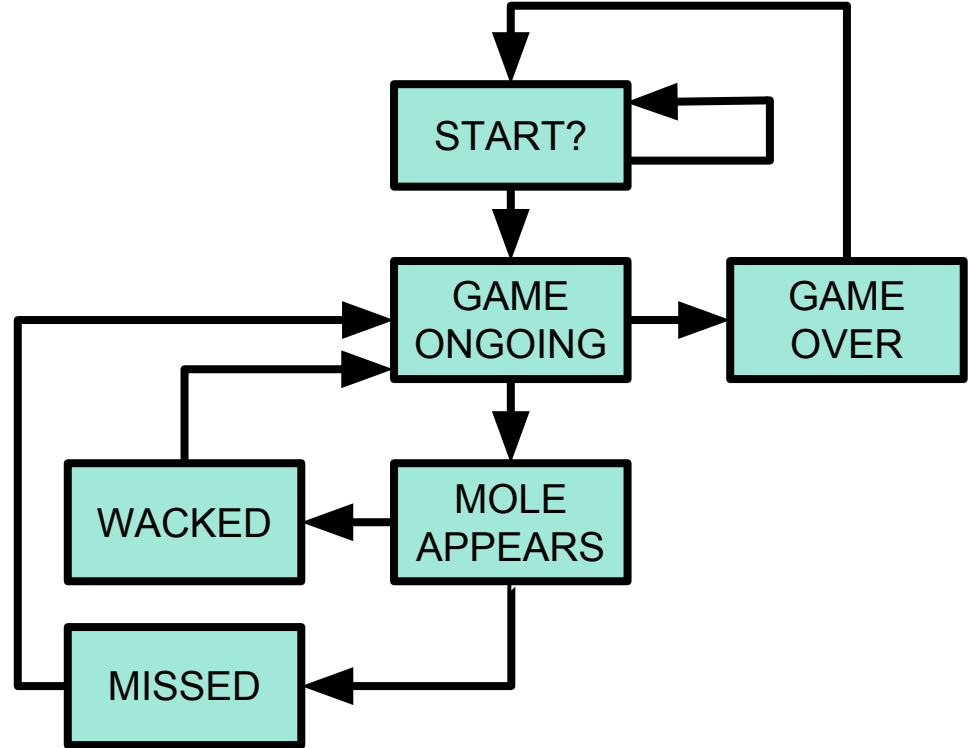
Manages Game State

Tracks Lives & Score

Controls Mole Timings & Locations

Updated by Foot Buttons

Outputs to Sound & Display



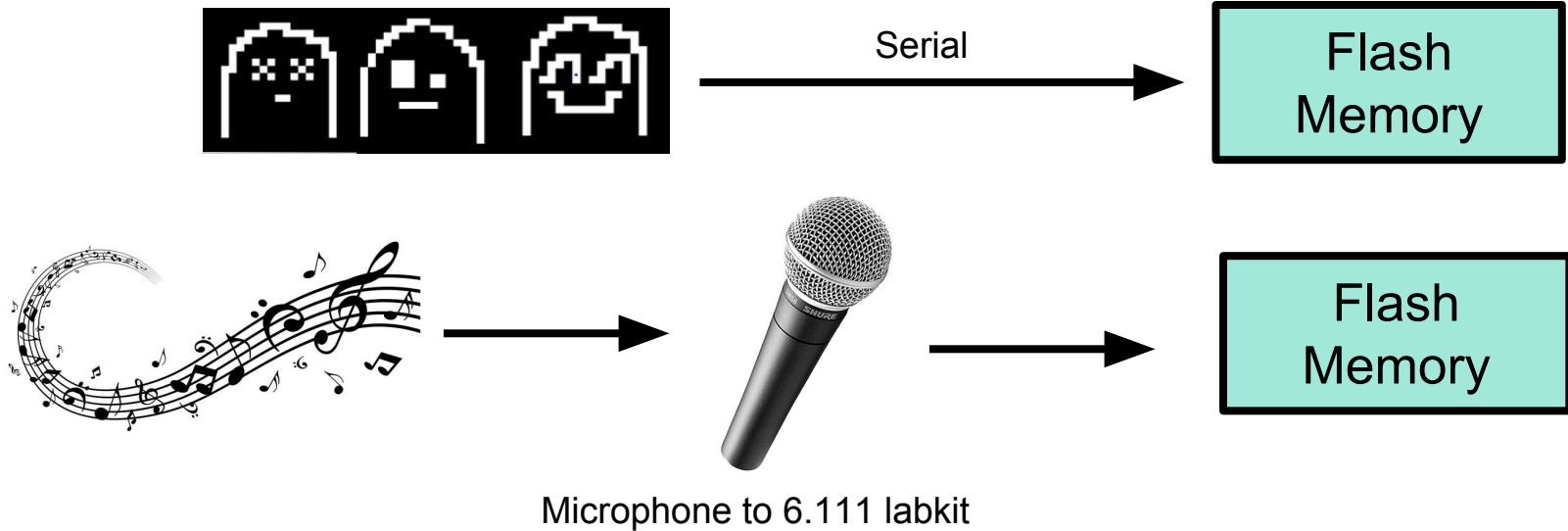
Preprocessing Images

- Images are preconditioned using photoshop (24-bit to 8-bit)



- Use MATLAB script to convert image to fpga-friendly format

Pre-Gaming: Image, Audio → Flash



Sound Module

- Game state input → address → retrieve audio data from flash
- Audio output to to_ac97_data
 - Background music
 - Sound effects for mole hit/miss
- Address output to game logic module
 - “timestamp” for mole pop-up



Graphics

- Load images from flash to BRAM right before game starts
- Outputs from game logic module determine
 - Which graphics to be displayed
 - Location of graphics on screen
- Additional graphics features to be added later



Game Features

- Base Goal
 - one mole with hit/normal/miss graphics
 - sound effects for hit/miss
 - background music
- Additional Features
 - Multiple moles
 - Gradual pop-up/disappearance of moles
 - Speed up game to real-time
 - Incorporate difficulty levels to the game

Projected Timeline

- Thur 11/9** In-Class Presentation
- Mon 11/13** Images converted to fpga-friendly format
Basic Game Logic Modules Created
- Fri 11/17** Flash Memory Storage Modules Created
Musically Synchronized Moles Module Created
- Fri 11/17** Submit Checkoff Checklist for Project
- Sun 11/19** Game Logic FSM States Finalized, Integrate with Sound & Graphics Modules
- Sun 11/26** Meeting to Determine Which Additional Features to Implement
- Mon 11/27** DDR Board Built
- Mon 12/11** Final Project Checkoff 4-10pm
- Tue 12/12** Project Demos and Videotaping
- Wed 12/13** Final Project Report Due @ 5PM

Questions?