PROJECT CHECK OFF MEETING

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DEMONSTRATION

Commitment:

- Successful Communication between two FPGAs:
- AC97 module: Samples audio signal at 48kHz with 12 bit depth and packets 3 by 12 samples in to 36 bit memory bus.
- ZBT module: Maintains 2 ^ 19 memory addresses
- Transmitter module: serially transmits the given parallel data, encapsulates it with packet address, header, CRC, and footer.
- Receiver module: receives serialized data and sends to CRC.
- FSM of Transmitter FPGA: Ensures correct behavior of Transmitter FPGA
- FSM of Receiver FPGA: Ensures correct behavior of Receiver FPGA including buffered (lagged) playback on receiving end

Note the correct behavior excludes interruption control

The Goal

- Communication between two FPGAs, Plus Interruption Robustness (Open Loop):

Demonstration of all the previously mentioned commitment, PLUS the system with interruption control.

Exhibition Steps:

Audio will be sent through the mic and the other side will be listening from the DAC out port of lab kit. Possibly will connect out port to a speaker. End-user will hear it with 5 seconds (subject to change) lag

To simulate interruption, we will simply unplug the fiber optic cable momentarily. The sound should be heard unless the interruption time exceeds lag time.

Far-Reach Goal

- Communication between two FPGAs, Plus Feedback Infrastructure:

Demonstration of all the previously mentioned modules PLUS the system with handling the re-sending process of data between FPGAs.

Exhibition Steps:

Audio will be sent through the mic and the other side will be listening from the DAC out port of lab kit. Possibly will connect out port to a speaker. End-user will hear it with 5 seconds (subject to change) lag

To simulate interruption, we will simply unplug the fiber optic cable momentarily. The sound should be heard unless the interruption time exceeds lag time.