Simultaneous 12-Lead EKG Recording and Display

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1 Overview

The goal of this project is to implement a 12-Lead EKG cardiac monitoring system similar to that used by prehospital EMS providers. Currently many EMS services use LifePak 15 devices or a Zoll equivalent. These are capable of displaying the patient's cardiac rhythm and printing a 12-lead analysis to paper. Our project will differ in its ability to display all 12 leads simultaneously and in real-time to the healthcare providers using this device. Using both analog and digital filtering will allow us to reduce both size and cost relative to current market options.

Our project will have 2 major parts. On the frontend, the device will have 10 physical EKG leads, which can produce 12 virtual leads. In order to provide the other components with an understandable heart signal, the input from the patient will be filtered with analog components prior to being read in by the ADC, which functions as the bridge between the two major pieces of the project. The digital backend will provide further filtering, specifically reducing high frequency noise, and will store each of the leads in memory. This means that a history of each lead is available at any time. Depending on user input, specific leads will be displayed on the screen for assessment by the user. If time allows, we will use EKG data to infer patients heart rate (pulse) by performing a FFT on the input signal.

2 Design

2.1 Analog Processing / Frontend

On the patient-facing side of the design are the analog devices that bring the heart signals into the labkit. These signals must be amplified before being read and saved to memory. Signals from the patient pass through an amplifier and a multiplexer to select the signals. In addition, the signals pass through a band stop filter to prevent line noise from distorting the signal. Each input has this band stop filter, but no further analog filtering. As discussed later in the Section 5, this is to prevent creating 10x as many filters as are necessary. The band stop filter however is made individually for each input. After the mux selects the correct signal, it reads into the device through the onboard ADC and saved to memory.

2.2 System Controller

At the center of our design is the system controller labeled EKG Main. The purpose of EKG Main is to be the center of communication between the user-inputs, display, frontend signals, and memory. EKG Main's communication with the user-interface is further discussed in Section 2.3. EKG Main's connection with the frontend signal processing unit is through the Recorder. EKG Main signals to the Recorder when to switch to the analog signal it should record next.

2.3 User-Interface

Our overall goal in designing the user-interface for the EKG is to allow the user to take advantage of all of the medical data provided by the frontend of our system. In order to achieve this goal, our EKG allows the user to select which waveforms he wants to see and display multiple waveforms on the monitor simultaneously. Additionally, the EKG displays the patient's current approximate heart rate.

In order to select waveforms to display, the user flips a set of switches, each corresponding to a particular waveform. EKG Main takes the set of selected switches and sends it to the Split Screen Logic along with information on where to find the selected waveforms in EKG Memory. Split Screen Logic receives the data of the selected waveforms from EKG Memory and responds to EKG Main with the pixel data dictating how to display the waveforms. This pixel data is then sent to the Display to be presented on a monitor.

In order to display a patient's heartbeat, the EKG has a Pulse Logic Module that receives the data of the strongest waveform (called v1) and processes it to find the patient's heartbeat. This heartbeat value is converted into pixel data in the Pulse Logic Module. The pixel data is sent to EKG Main, which is then sent to the Display.

Display is a typical display module that receives pixel data from EKG Main and sends it to a monitor over VGA.

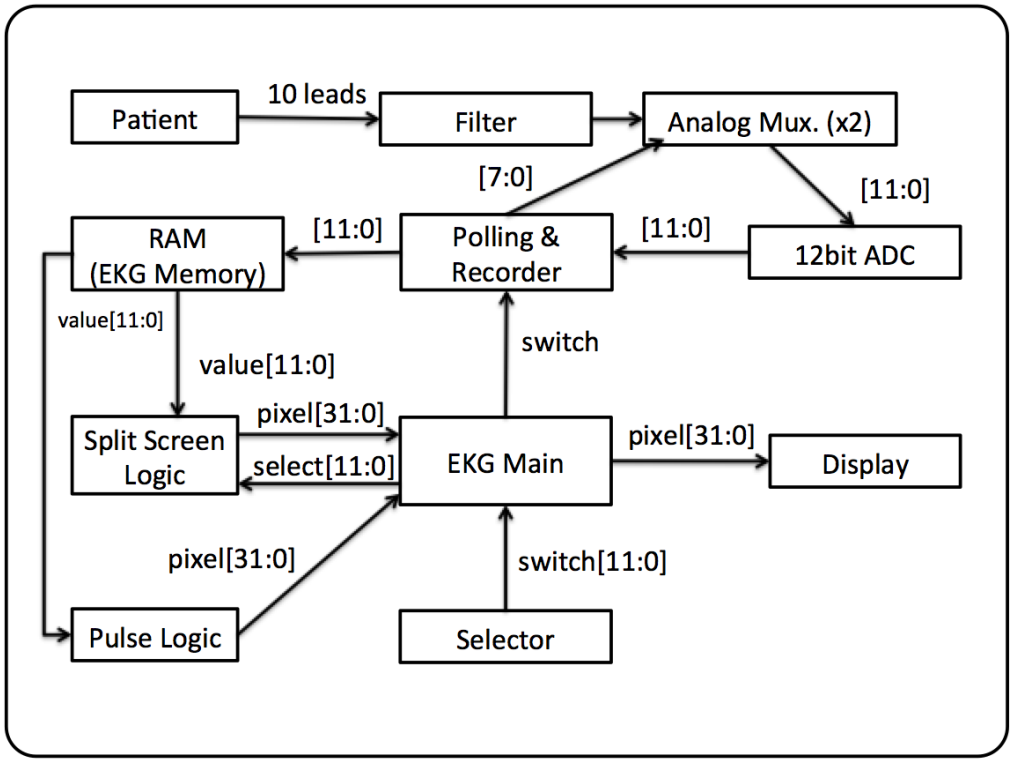

Figure 1: System Block Diagram

3 Implementation

3.1 Analog Processing

The analog processing of the patient's heart rhythm is designed with a combination of several elements. First, EKG leads and lead ends bring the signal to the LabKit. The set of leads consists of 10 wires, one of which is grounded. The remaining 9 leads are then placed into 9 separate notch filters as shown below. Since the most significant source of noise in the project is 60Hz line noise, each input signal is filtered by a notch filter set to 60Hz prior to being an input to an analog multiplexer. The multiplexer is controlled by the backend and selects which lead is currently being fed to the amplifier.

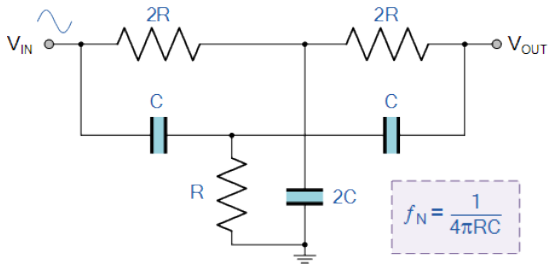

Figure 2: Notch Filter

For conversion to a digital signal, the heart signal (order mV) needs to be amplified in order to be read properly by the ADC. This is done using a Texas Instruments medical grade instrumentation amplifier. The benefit of the instrumentation amplifier is that its multiple amplifier design results in high gain with low DC offset. This is ideal for our use. In addition, the selected package allows for adjustment of the gain by changing a single resistor. This is ideal for initial testing and debugging. A schematic of an instrumentation amp is shown below.

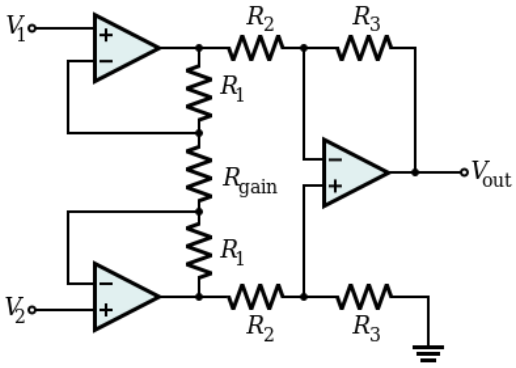

Figure 3: Instrumentation Amplifer

In addition, several of the Leads are not referenced to ground, and are instead referenced to each other. Therefore, we use two separate analog multiplexers so that we can individually select the two leads that are inputs to the instrumentation amp.

3.2 ADC

After being filtered, selected, and amplified, the differential voltage measurement between the two physical leads are read into the digital system. This is done using the ADC onboard the Nexys 4 FPGA board. This ADC offers 12-bit readings at a maximum rate of 1 million samples/second. This sample rate is far greater than is needed to accurately reproduce any one lead. However, we instead are reading data for all 12 virtual leads using this ADC. Using 1MSPS as specified, we expect at most ~80kSPS if we are to poll through the physical leads needed to create the virtual leads. 80kSPS is also well over the sample rate required to sample any one lead. Therefore, we believe we can reasonably sample all needed data using a single ADC. In order to read all 12 virtual leads, the recorder module sends the corresponding signals to the Analog Multiplexer select lines to select the correct lead and append the value to the memory bank corresponding to the correct virtual lead to be displayed.

3.3 EKG Main

EKG Main takes as input 12 bits of switch data from the Selector Module and two 32-bit pixel data. EKG Main outputs the selector data to the Split Screen Logic Module and the bitwise OR of the two inputted pixel data to the Display Module. Additionally, EKG Main tracks when the Recorder Module should switch between waveforms to record and outputs a switch signal to the Recorder Module.

3.4 User-Interface

For the Selector Module, the EKG utilizes twelve of the switches on the Nexys4 corresponding to one waveform each. Every clock cycle, EKG Main stores the lower twelve bits of the switches.

For the Split Screen Logic Module, its inputs are a 12-bit data bus from EKG Main corresponding to which waveforms should be displayed and a 12-bit value from the EKG Memory corresponding to the last recorded data from a particular waveform. Within Split Screen Logic, each last 3 seconds of waveform data is stored in registers. Each clock cycle, Split Screen Logic receives this new data value from memory and updates its own register corresponding to the waveform that was just updated. Additionally, Split Screen Logic takes the 12 bits of selector data and selects which data values it will display. Based on the number of 1's in the 12-bit data bus, Split Screen Logic creates that number of screen long blobs to display the waveforms. Considering the monitor is 1024 pixels wide, each displayed data's pixel y-value is calculated from every third data value from the waveform register, resulting in a 1000 pixel wide display per waveform. The x-value of each subsequent data's pixel x-value is just incremented from the previous displayed pixel's x-value. Every 65 MHz clock cycle (assuming XVGA), a 32-bit pixel value is output to EKG Main based on hcount and vcount.

For the Pulse Logic Module, its input is a 12-bit data bus from EKG Memory. A pulse of a heartbeat appears when high voltage values are read. Pulse Logic takes this input and updates its own register of data values corresponding to the v1 waveform. Then, Plus Logic calculates when in the last 3 seconds a pulse has occurred. Subsequent high values imply the heartbeat is of the same pulse so Pulse Logic waits for a sequence of low values to calculate the next pulse. The number of pulses then multiplied by 20 to get an average heart rate. The number of pulses is then converted into a blob value to be displayed in the top right of the monitor. Every 65MHz clock cycle, a 32-bit pixel value is output to EKG Main.

The Display Module take a 32-bit pixel value from EKG Main as an input and sends pixel data over the XVGA cable. The display monitor for the EKG supports a 1280x1024 display. The EKG Display Module resolution is 1024x768.

4 Testing

4.1 Analog / Frontend Testing

In order to test our implementation, we will first use test benches within the development environment before deploying the code to the actual labkit / Nexys 4. This will allow us to know our Verilog is free from gross errors prior to implementing it into the rest of the system. After verifying initial functionality, we will use test signals to ensure the digital systems are working. To do this, we will use an arbitrary waveform generator that produce varying signals to feed into the analog multiplexer. This will allow us to bypass the hardware filtering and amplification and directly test the lead multiplexing, user interface and display. After verifying that those stages work, we can implement the hardware interface to the patient, knowing that the following processing steps are functional.

4.2 User Interface / Display Testing

To mimic waveforms for testing on the user interface side, we will use both an arbitrary waveform generator and a series of 3000 data values representing different waves generated by Matlab. To test the Split Screen Logic Module, we will input 12 Matlab generated waveforms and ensure that all 12 are displayed correctly on the monitor. Different types of waveforms will be used for testing to ensure correctness of the display. To test the Pulse Logic Module, we will input a Matlab generated waveform and ensure the correct number of peaks in the waveform are counted and displayed. Additionally, we will generate waveforms with different numbers of peaks to ensure the functionality of the module.

5 Technical Challenges

The biggest technical challenges here are two-fold. First, we must implement the waveform displays such that they are modular and resizable. For example, if the user selects to view only one lead, the waveform should take up nearly the entire display. The lead should also be centered and have the appropriate line thickness. Now, say the user wants to view all 12 leads simultaneously. The top, bottom, and sides of each waveform must be calculated individually. In

addition, the line thickness and center of each lead should be adjusted such that the waveforms stay within their predefined boundaries but are still visible to the user.

Additionally, we will need to do significant filtering digitally that would generally be more efficient to do in the analog domain. This is because since we have so many leads, it would be impractical to make 10 low pass filters and 10 high pass filters for each lead prior to sending the signals to the multiplexer. In addition, we can't place just one filter behind the multiplexer because the polling nature of the sampling will introduce high frequency noise.

6 Timeline

Week of	10/31	11/7	11/14	11/21	11/28	12/5	12/12
Block Diagram	Both						
MUX Select / ADC Input		Stone					
Split Screen Logic / Display		Jeremy	Jeremy				
Analog Filtering			Stone				
Proof of Concept				Both			
Advanced Filtering					Stone		
Pulse / HR detection					Jeremy		
Debugging / Finalization						Both	
Final Presentation							Both

7 Required Resources

Other that the components available in the lab, we will need a medical grade instrumentation amplifier, a 12-lead EKG cable, EKG lead ends, and 2 analog multiplexers. The instrumentation

amp and analog mux will be purchased from Digikey and the medical equipment will be purchased online from a medical supplier.

8 Conclusion

The Simultaneous 12-Lead EKG is an interesting and important project because it is directly beneficial to patient care by helping EMTs diagnose cardiac problems. The improvement of our system is the ability for our EKG to display twelve leads simultaneously. However, the main challenge of our project is the task of displaying all twelve leads clearly. Through this project, our team is looking to learn and gain experience in multiple techniques of signal processing and display technologies.