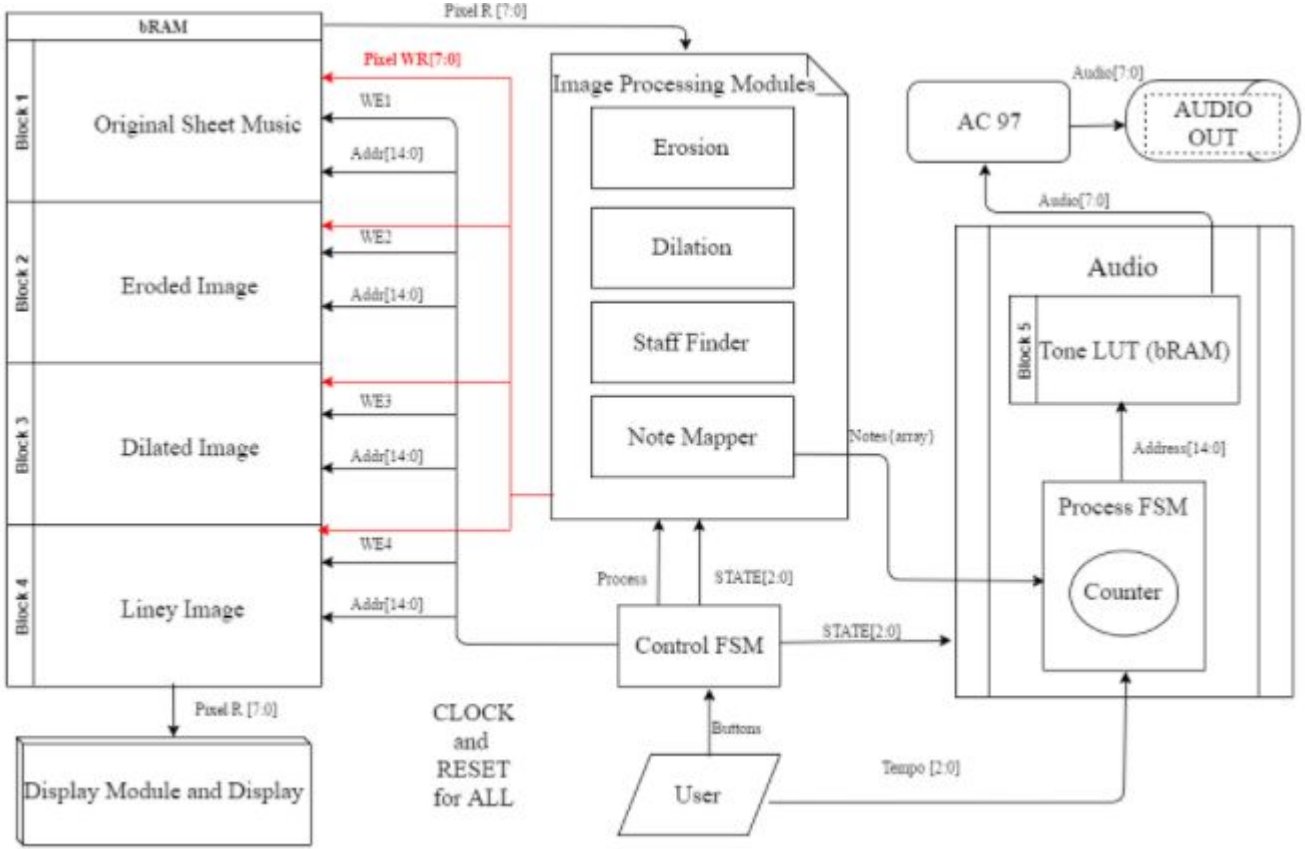
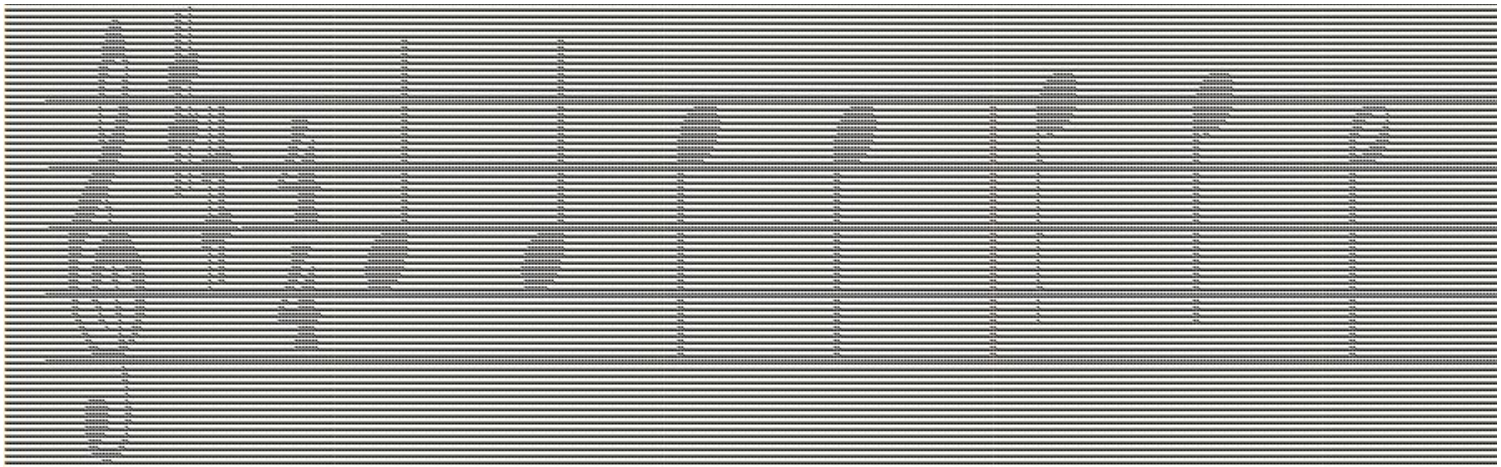
FPGA Beethoven

Henry Love & Mark Yang

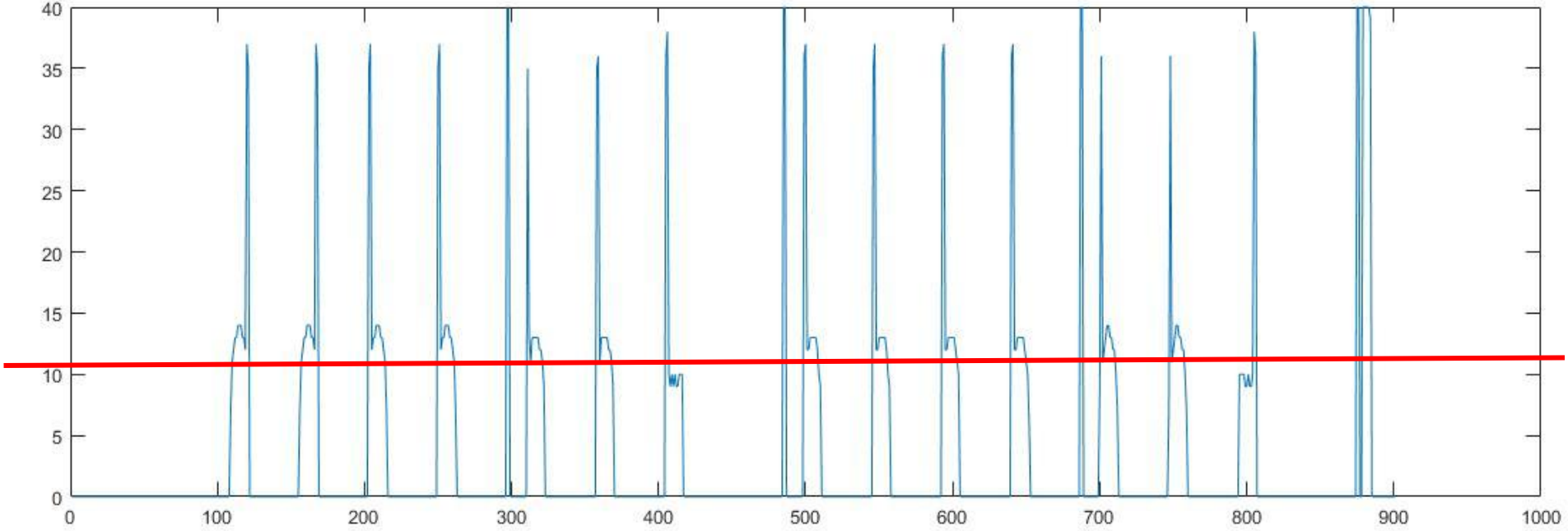
Block Diagram



.coe File

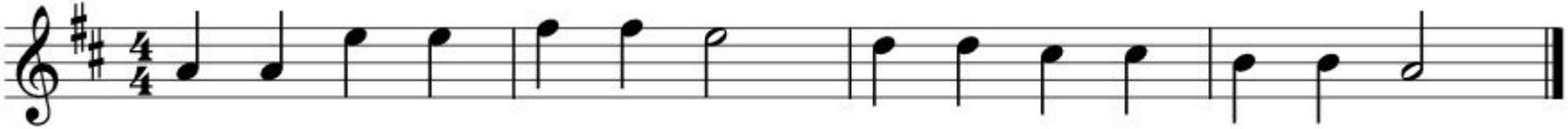


Note Recognition

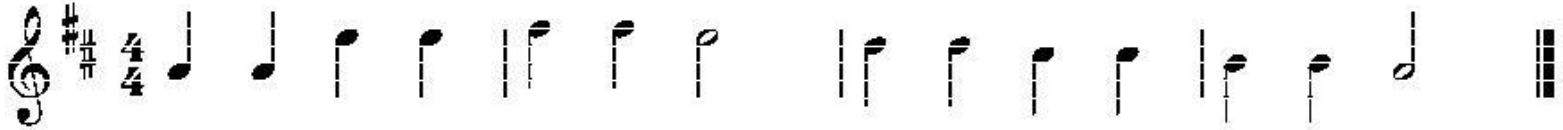


Pixel integration and thresholding

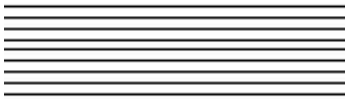
Image Processing



Line filtering



Line detect



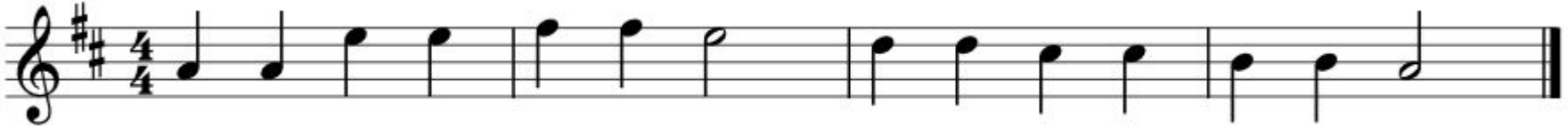
```
score =

    18    23    28    33    37    42    47    52    57

>>
```

Erode and dilate

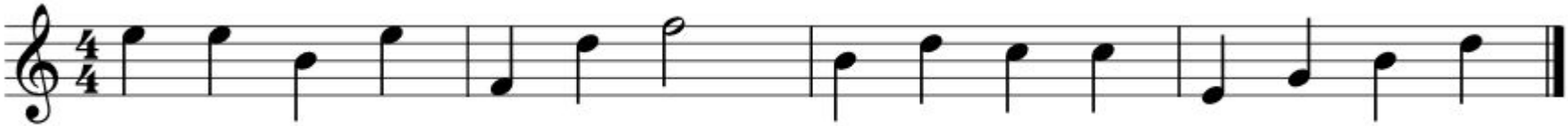
Note detection with Erosion and Dilation

```
note =

    18    18    23    23    23    28    28    33    33    37    37    42    42    42

xCoord =

   325   372   217   264   418   512   559   606   653   715   762   123   170   808

order =

    42    42    23    23    18    18    23    28    28    33    33    37    37    42
```

Note Detection



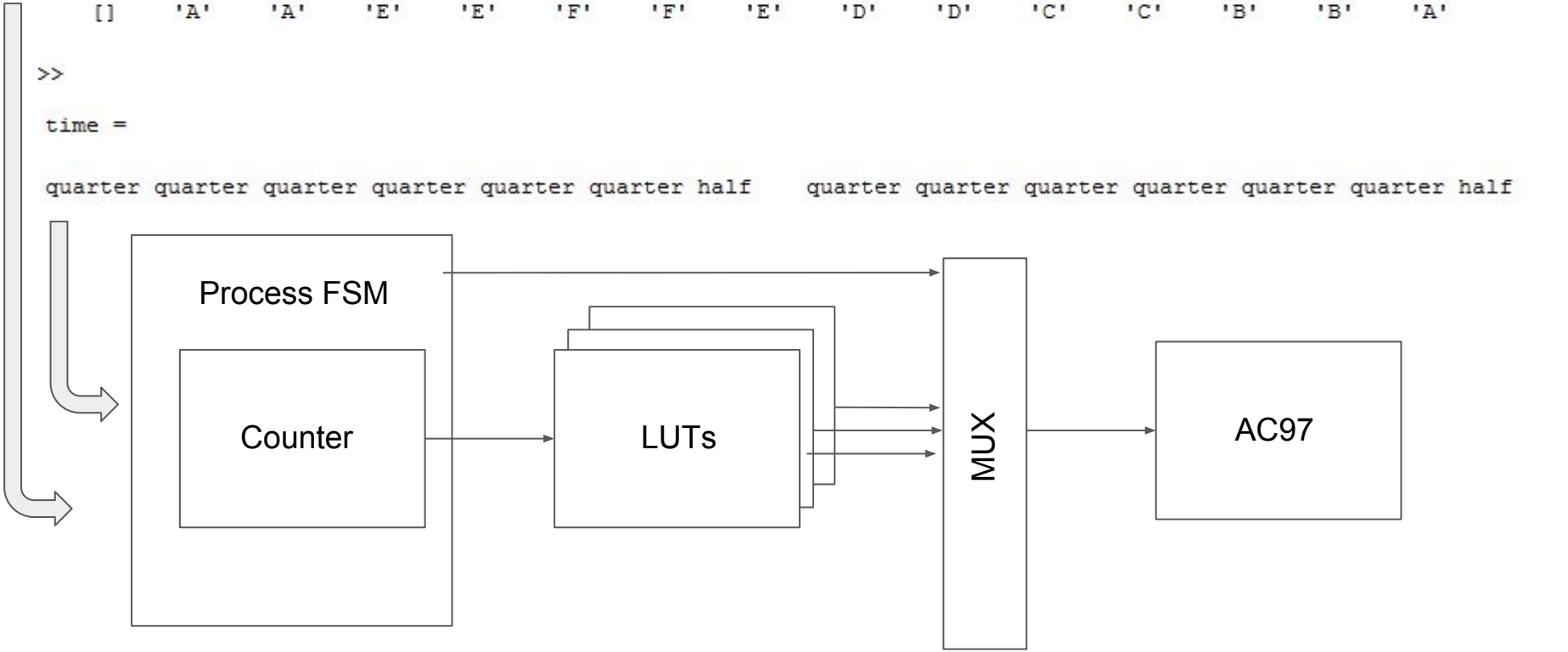
```
actualNotes =

    []    'A'    'A'    'E'    'E'    'F'    'F'    'E'    'D'    'D'    'C'    'C'    'B'    'B'    'A'

>>
```



```
actualNotes =

    []    'E'    'E'    'B'    'E'    'F'    'D'    'F'    'B'    'D'    'C'    'C'    'E'    'G'    'B'    'D'
```

Sound LUT and AC97

```
actualNotes =

    []    'A'    'A'    'E'    'E'    'F'    'F'    'E'    'D'    'D'    'C'    'C'    'B'    'B'    'A'

>>

 time =

 quarter quarter quarter quarter quarter quarter half    quarter quarter quarter quarter quarter quarter half
```



Schedule

	Essential for proof of concept
	If time permits

	10/31	11/7	11/14	11/21	11/28
Bring online all provided modules					
Matlab proof of concept functional					
Implement memory structure in Verilog					
Implement erosion & dilation in Verilog					
Implement staff finder in Verilog					
Implement note mapper in Verilog					
Implement control FSM in Verilog					
Bring first version online					
Final Debugging					
Allow for different key signatures and cleff					
Implement camera vision					
Implement better note detection algorithm and account for different time signatures					