6.111 Project Checklist
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- the commitment: the minimum that you hope to achieve; shows an adequate understanding of digital systems and Verilog. Complexity typically twice the complexity of the car alarm lab. Project grades are typical 10-19 out of a max of 35.
- the goal: a fully functioning project meeting all the checklist items in this section. Demonstrates a superior understanding to digital systems and implementing complex systems - perhaps with multiple time domains, interface to external devices, flash memory, audio, etc. The implementation goes beyond what was in the labs. The project grades range from 20-29.
- stretch goal: a top notch project that really stands outs with complexity, innovation and risk.

Checklist

Commitment

1. Working Play/Record FSM - Priya
    a. able to play eight different audio tones and record reflected signal in memory up to 14,000 Hz
2. Able to read recorded signals and generate compensation values for each frequency -Priya
3. Instantiate ADC and DAC for audio IO -Alex
4. Find suitable microphone and speaker -Alex
5. Working FFT and IFFT -Alex
6. DSP is basic compensation (multiplication) -Alex
7. Explore lower bound of frequency bin amount - Alex

Goal

1. DSP has bass, treble, EDM, classical - Alex
2. Plot transfer function of room on screen -Priya
3. store room characteristics in memory to be applied to music with switch -Priya
4. increase number of tones from 8 -Priya
5. Test multiple speakers -Priya and Alex

Stretch

1. update transfer function display in real time -Priya
2. emit all tones in real time and take FFT of them to generate transfer function -Priya
3. use labkit switches to generate tones and mix with music - Alex

--nexyses 4 display code on website