Delta-Sigma Heart Rate Monitor

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1 Overview

In the realm of medicine, doctors try to use non-invasive methods to measure vital signs. These methods which involve the use of pulse oximetry for heart-rate are often expensive, involve big bulky machinery, and display a normal waveform. There are other devices on the market that also measure heart-rate but they cannot display an actual heart waveform. This final project aims to make a heart rate monitor that allows one to measure their heart-rate as well as see their heart-rate waveform.

There are two important modules for this project. First the Delta-Sigma analog to digital converter, for which this project is named after, will generate a certain number of bits from an analog signal provided by a pulse oximetry probe. From these bits, heart-rate data and heart-rate waveform can be calculated and displayed. The second important module is the graphics module which is responsible for creating control signals that will be used to display visuals on a monitor. Ultimately, the project will be take in a person's heart-rate and it will be able to display it on a monitor.

Stretch goals include having sound to accompany the displayed waveform, the implementation of noise shaping which will allow for more generation of bits, and better data-point visual representation. The ideal outcome of this project would be to be able to use this heart-rate monitor almost anywhere as long as there is an FPGA, the probe circuitry and a monitor.

2 Design

2.1 Project Overview

The project as a whole can be modeled as 6 major block components as shown in Figure 1; these blocks are the analog circuitry block, the Delta-Sigma analog to digital converter (ADC) block, the digital signal processing block, the graphics block, the character storage block and the VGA block.

The pulse oximetry probe will be used to collect data that will passed into analog circuitry to be filtered. This filtered signal will then be the input to the FPGA for 1 bit sampling and higher precision reconstruction. The high precision digital signal will then be processed by the Fast Fourier Transform (FFT) module that will help to identify the heart rate. The graphics module will take the heart rate data and while interacting with the character storage module, it generate a control signal for the VGA module that will display the waveform and associated data on screen.

Joe and Hugo will be dividing the project into two sections: acquiring and displaying data. Joe will work on the acquisition of data implemented with the delta-sigma algorithm. Hugo will be in charge of the filtering of the data and displaying it on a monitor.

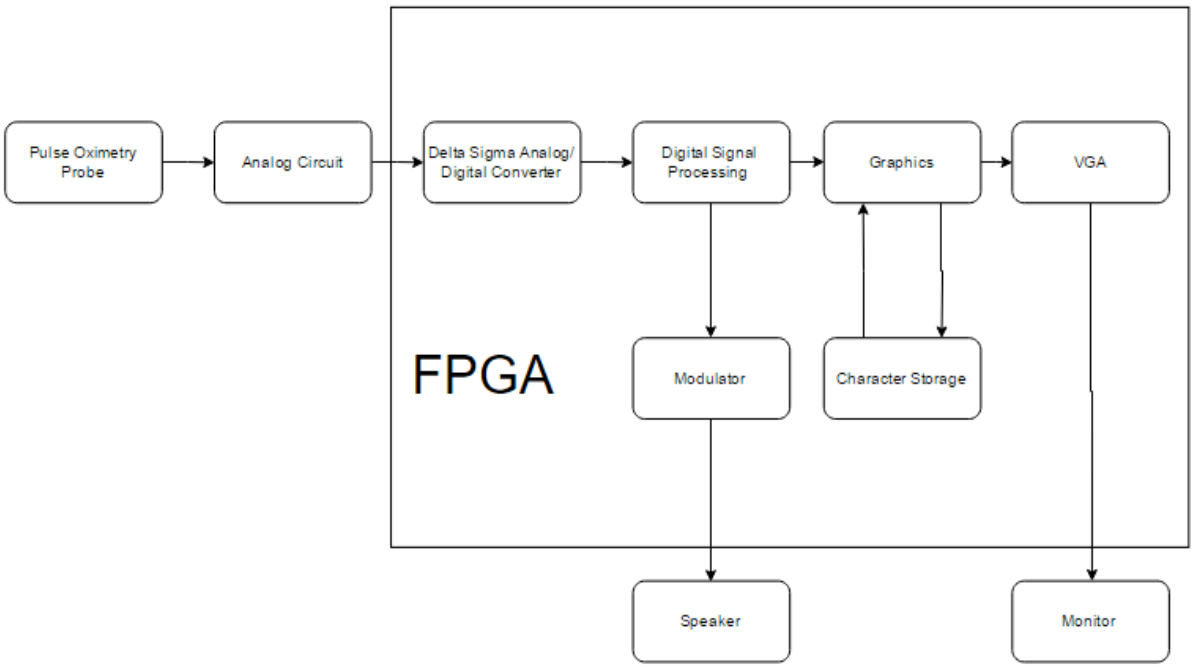

Figure 1: The high level design of the system

2.2 Design Decision and Motivation

The primary motivation for this project was to use methods learned in several classes such as 6.341 and 6.011 as well as implement everything learned in 6.111 to build a graphic representation of an input waveform. At first this was supposed to be an oscilloscope but after viewing doing some calculations, it was concluded that building an oscilloscope from an FPGA was not too feasible due to the high speed needed for sampling and transfer of data. A slower input signal was needed and it seemed the obvious choice for this was heart-rate.

3 Implementation

This section explains more of the details of the system and verbalizes the block diagram shown in Figure 1.

3.1 Pulse Oximetry Probe Block

The pulse oximetry probe is a physical component that clips on to a patient's finger. It works by working out the oxygen saturation by comparing how much red light and infrared light is absorbed by the blood when blood is pumped through a patient's body. A photodiode then

collects the amount of light transmitted by the red and infrared LED. Calculations can then be done to generate a waveform signal. The pulse oximetry used will be provided by Gim Hom for this project. This signal will then be passed on to our analog circuitry for further processing.

3.2 Analog Circuitry Block

The purpose of the analog circuitry block will be prepare the waveform signal for digital conversion so it can be processed by the FPGA. This will be done by implementing three separate analog circuits.

First noise needs to be limited and bandwidth has to be determined. Since the signal being dealt with is a heart-beat signal, a 2^{nd} order low pass filter is needed to eliminate 60 Hz noise that comes from the outside world. In the end we should have a passband from DC to about 10 Hz.

Second our low-passed filtered waveform will be sent to a comparator circuit where a 1 bit transistor-transistor logic (TTL) voltage signal will be generated. The comparator is a prepackaged chip that can be bought separately with the project funding for no more than a few dollars.

Lastly, the FPGA can only accept signals of certain voltages. To avoid this issue, a TTL level shifter will be implemented to avoid any input discrepancies. Depending on the comparator used, this stage may not be required.

After this last analog circuit, the signal will be given to the FPGA where it will go into the ADC module.

3.3 Delta-Sigma Analog to Digital Converter Block

This Analog to Digital Converter (ADC) block a major block module for this project because this module will generate multiple bits that which are essential to displaying the heart-rate information on the monitor.

The ADC assumes that the incoming signal is band-limited, which is guaranteed by the low pass filter in the previous stage. This signal is then sampled at a low precision well above the target frequency. By using heart-rate as the input signal, this is easily achievable by the FPGA.

Afterwards the signal is then passed through a high precision digital filter, then decimated down to a much lower sample rate. This process allows for trading of high frequency sampling for high precision generation of bits. The number of bits depends on the oversampling rate and as of now, the expected amount of bits generated is 6 without implementation of noise shaping which is a stretch goal.

With noise shaping, the signal to noise ratio of a signal is raised meaning that more noise is eliminated. Depending on the order of noise shaping we can add a certain number of bits of

precision. In this project, noise shaping higher than 3rd order will not be pursued as at that point, the number of generated bits remains constant.

3.4 Digital Signal Processing Block

The Digital Signal Processing (DSP) block has the important task of interpreting what is the actual heart-rate of the patient by looking at major frequencies. This will be implemented using a Fast-Fourier Transform (FFT) module which will continuously be receiving and operating on data from the ADC. The frequency data output from the FFT module will then be used to identify the heart rate of the patient based on significant frequency components.

Another module within the DSP block, the Analysis module will be responsible for identifying the primary frequency component, declaring that as the heart-rate and recording it in a time series of heart rate data which will then be passed on to graphics along with the original data that was analyzed.

3.5 Graphics Block

The Graphics block is another major block for this project because ultimately it creates the signals that the VGA module will use to display pictures to the monitor. The way the graphics module works is that it takes data from the DSP block and it generates the output necessary to allow the VGA module to generate the heart-rate data waveform on the monitor.

Since the data that is being received are just data points, the graphics block has to connect the data points. Using interpolation that can be called Manhattan style, a continuously connected waveform will be generated that will be converted into a control signal that the VGA module needs to output a picture.

The graphics block will also make a call to the character storage block to obtain the correct characters to display heart-rate in fancy numbering and lettering. This component will also be converted into a control signal that will be sent to the VGA module.

3.6 Character Storage Block

The characters that the FPGA can display are not so interesting. The character storage module will add interesting lettering and numbering that can be exchanged so it will be easier to read information on the display.

This block will take pixel indices as an address and output an opacity bit that will indicate whether to color the indexed pixel to match the character color or the background color.

3.7 VGA Block

The VGA block is necessary to actually display picture on the lab monitors. It does this by taking in a 12 bit color signal and associated VGA control signal and with those it generates a VGA compatible Digital to Analog Converter (DAC).

4 Timeline and Testing

Figure 2 is a Gantt chart showing the proposed schedule for this project. The following section is dedicated to elaborating on the steps in Figure 2.

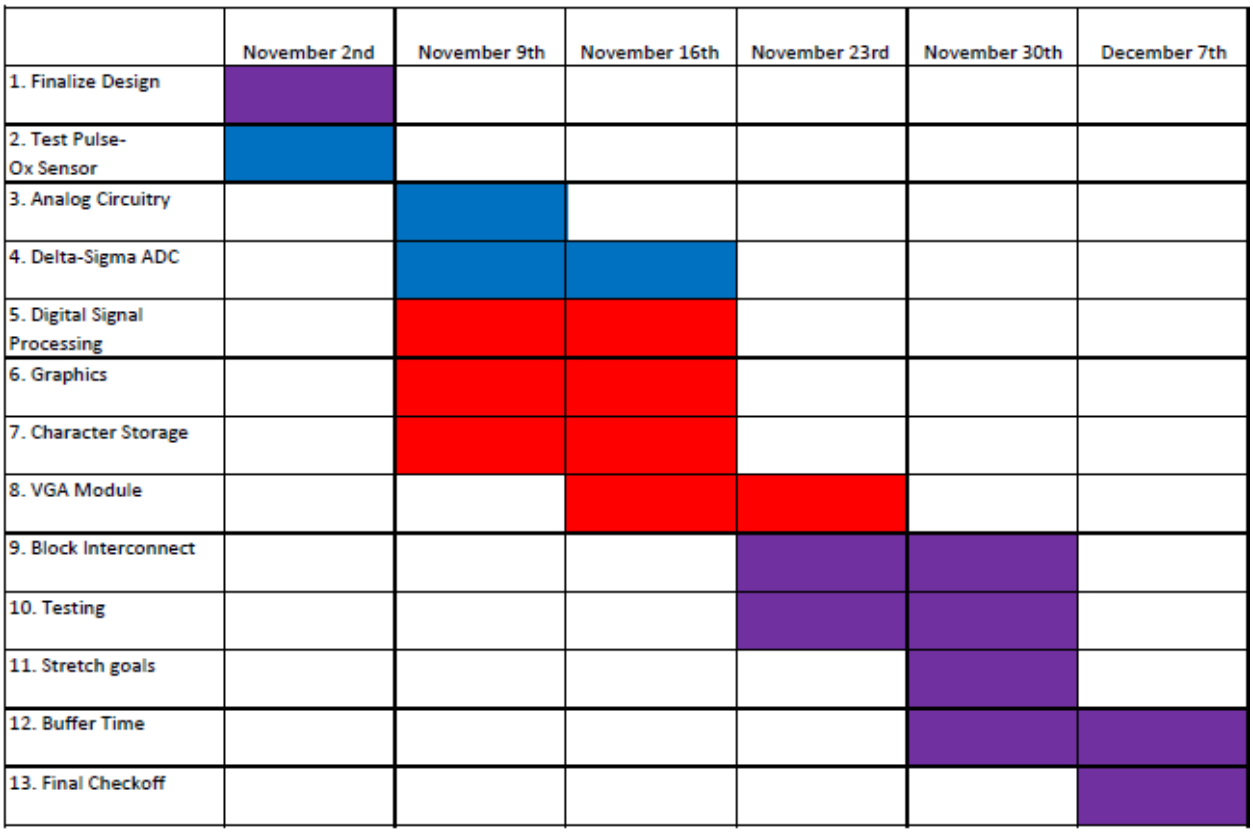

Figure 2: Gantt Chart of Proposed Timeline

Elaboration and Testing Methods

1. The pulse oximetry probe testing was completed for the team during the initial feasibility conference with Gim Hom. No further testing is required.

2. The analog circuitry block has three components, all of which can be tested by connecting the circuit to a signal generator and checking the output with an oscilloscope.

3. The ADC block can be tested using a signal generator and a logic analyzer. Simply putting in a known waveform and observing the same waveform on the logic analyzer will indicate that the ADC block works.

4. The DSP will be tested by first using a sine wave as data. After being able to identify the primary frequency, and the heart-rate data is ready, two measurements will be taken. One measurement will be with the pulse-ox probe and the other will be a normal heart-rate measured. The FPGA will use the 8-bit segment display to demonstrate the correct value.

5. The Graphics block will be tested by displaying the waveforms on the lab monitor. At first this will be using a sine wave to ensure that interpolation can be performed on the data.

6. The Character storage block will be tested once the graphics module works. This will be tested by displaying one character on the monitor at a time until all characters needed are displayed on the screen.

7. The VGA module is one of the first components that will be tested. It is necessary to test the signals using the VGA module to ensure the monitor is displaying the correct images.

5 Resources

This project will require some additional components aside from the FPGAs and monitors provided in lab. We will need some analog chips which we can obtain from EDS or if not available from Digikey. The pulse oximetry probe that will be used will be provided by Gim Hom. Our team has experience using all these items so we should have no problems implementing these components into our project.

6 Stretch Goals

If time permits, we plan to implement the following features:

1. Modulation block module so sound can be heard alongside the visual waveform.
2. Noise shaping for the ADC block. This will allow us to increase the number of bits that can be generated and improve the waveform precision.
3. A linear interpolation method that will increase the crispness of heartrate signal being output.

7 Conclusion

The Delta Sigma Heart Rate Monitor is a project that efficiently combines our interests into one. Having taken different classes such as 6.011 and 6.341, it will be interesting to see how we can implement our theoretical knowledge to demonstrate on a visual level. Just generating a heart-rate signal, even if it is still, will be very exciting. Finally, this project will give us new experiences that will allow us to go and build more things with FPGAs for future projects.