6.111 Self-parking Car Checklist

1. Sensor Block (Frank Ni)

a. adc and sensor interfacing (hardware)
- -multiplex ADCs using chip select
- -wire chips and circuit
- -test sensor response

b. divider module (Verilog)
- -create different clock speeds for ADC read

c. readSensor (Verilog)
- -generate signal for reading the ADC by giving it enough conversion time
- -serialize reading the ADCs by cycling through each of the four
- -collecting all four sensor data then passing it on to next block

d. calcDistance (Verilog)
- -convert voltages to distance by taking inverse of the voltage

2. Control Block (Frank Ni and Kevin Hsiue)

a. FSM self-parking module (Verilog)
- -create state transition diagram for parallel parking
- -determine how vehicle should stop
- -deal with pre-defined space
- -deal with variable parking space

b. Xbee control (if time permits) (Verilog/Hardware)
- -Module for receiving data and communication with vehicle
- -wireless control

3. Motor Block (Kevin Hsiue)

a. PWM module (Verilog)
- -Create a PWM waveform with a duty cycle as parameter
- -determine maximum frequency for motors

b. Divider module (Verilog)
- -Divide the clock into different frequency

c. Clock module (Verilog)
- -Generate a clock signal from the divided clock

d. LM18293 and motor interfacing (Hardware)
- -Get the motors turning and being able to control all wheels
- -Determine battery supply for motors
- -Protection circuitry for motor back drive current

Miscellaneous:
a. Rewrite UCF file and create template labkit.v file for Basys 2 FPGA
b. Create parking environment with cardboard
c. Construct chassis and mount boards and sensors