Abstract

The MIT-led TESS and REXIS collaborations intend to build two satellites based on the same image-capturing platform composed of a custom charge-coupled device (CCD) array designed to detect X-rays from distant stars and asteroids and an on-board FPGA for image preprocessing and data storage. While both of these projects have been in development for several years and some hardware has been designed and constructed, the FPGA code that manages data collection and processing has not yet been written. This project will first implement a digital system that establishes the data processing stream for TESS. This starts with 10 images stored on a CompactFlash (CF) card that represent actual data collected by the satellite. The 10 images are stacked on each other to produce a composite image and then using a known list of coordinates in the image small portions (referred to as “postage stamps”) are then cropped out and stored on the CF card to send out later for data analysis. Controlling these modules is a user-interface composed of available switches and buttons on the 6.111 labkit (or a separate development board; see Prior Work section for more information). Once this basic functionality is achieved, additional modules that connect the prior work on this project to the new work implemented here will be constructed. These include a module to receive and store on CF live image captures from TESS' CCD array and a module to reconstruct the images before passing them on to the data processing routines. It may also include modules to interface the FPGA to a computer through a serial protocol or the REXIS data processing module.

Prior Work

Much work has already been done on the TESS image capture and image processing hardware. Referring to the “Prior Work” section in the block diagram, the physical hardware necessary to capture the image has already been designed and constructed. TESS features six 16 megapixel (MP) CCD arrays, although for the purpose of this project we will only consider one array. In order to show proof of concept that these camera elements work and can produce usable images the array is connected to a Xilinx ML507 development board featuring a Virtex 5 FPGA. Code has been written for this board that grabs a frame in CameraLink format and produces a bitstream into the FPGA that can be used to store the image for later use.

The ultimate goal of this project is to complete this design, although that will not occur before the final project deadline. The existing code must be instantiated on the board to grab the image and stored on a CF card such that the image can be reconstructed by the FPGA at any time. After that, the image must go through the data processing routines described above, then sent to an external computer for data analysis. Ideally, all of this would be implemented on the ML507 board since it will be used beyond 6.111, but due to a lack of infrastructure and support this is not realistic. Instead, development on modules responsible for connection of prior work to the focus of this project will occur in parallel as time allows. This would include the aforementioned modules that store images taken with the actual TESS camera as well as reconstructing them on demand. These images could then be processed in the same way as the dummy images in this project.

Project Modules

This project will focus development on the 6.111 labkit so that the code can be ported to the ML507 board at a later date. Referring to the “TESS Data Processing Chain” section of the block diagram, the following modules will be implemented on this labkit:

- CompactFlash Memory Controller: The memory used for this module is CF as opposed to a BRAM implemented on the FPGA or the labkit's ZBT RAM because it is far more realistic and

useful to the TESS project. TESS' CCD arrays have a resolution of 16MP with each pixel containing four channels of data. One channel is the actual pixel intensity, represented with 18 bits of data. The other three channels contain information relating to where the pixel resides in the entire array but because they do not contain actual data they can be discarded. This makes each image about 34.3MB in size (at a minimum), far too large to store on ZBT or BRAM. In addition, implementing a CF controller should be instructive in interfacing the FPGA to a memory architecture. The throughput of this module ideally will meet the TESS specification of 16MB/s/camera (TESS has six cameras). Because this is only a proof-of-concept demonstration, we will only design around the throughput for one camera.

- Frame Stacking: This module reads in 10 dummy images from memory and “adds” them together to form a 10-layer composite image. Since each data has 18 bits of information per pixel the composite image will have 2^18 * 10 = O(2^22) possible values for each pixel. Effectively, we compress 10 18 bits/pixel images into one 22 bits/pixel image. The stacked image will also be stored in memory so as not to destroy the original data.

- Postage Stamp Clipping: TESS is only interested in analyzing data from stars that are believed to be harboring orbiting exoplanets, and since space is mostly empty most of the image data is not useful. There is a list of known stars that TESS will study, and this star catalog can be written into the FPGA and used to cut out the useful parts of the image that correspond to where in the sky the image was taken. In this project a list of dummy “star locations” will be hard-coded into the FPGA (although in reality this may be loaded in from memory) which stamp to clip will be determined by user input through the User Interface module.

- User Interface: The user-interface module will stand in for the input data stream from an external computer that runs TESS' data analysis. The computer requests a postage stamp to analyze and in this case the labkit switches will serve as the input request. By setting the switches to any eight-bit binary number up to 64 different postage stamps can be clipped from the same composite image. The labkit switches will also be used to switch the video output to each stage of the image processing pathway.

- Video Out: While not necessary for the TESS project this final project needs a way to actively display what the hardware is doing. To that end a video display module will be written in order to forward the images to a projector so that the class may see each stage of image processing.

If there is extra time the following modules may also be implemented:

- Output Interface: Since the FPGA must communicate with an external computer, one of a number of communication protocols (USB, RS232, SPI, etc) may be implemented in order to connect the two devices and transmit/receive data. It is currently unspecified which protocol will be necessary for TESS.

- Live Image Capture and Reconstruction: There is existing code (written in VHDL) that will capture a live image from TESS' CCD array and process it into a bitstream that can be stored in memory. This module would instantiate that code and use the CF Memory Controller to store

this image in memory. On a user request this module would reconstruct the image from memory and push it to a computer or projector using the Video Out module and/or send the reconstructed image through the data processing pathway.

- REXIS Data Processing: This module(s) would implement the REXIS image processing pathway, which is different from TESS'. TESS examines bright stars for the existence of exoplanets while REXIS takes images of asteroids in order to determine their chemical composition.

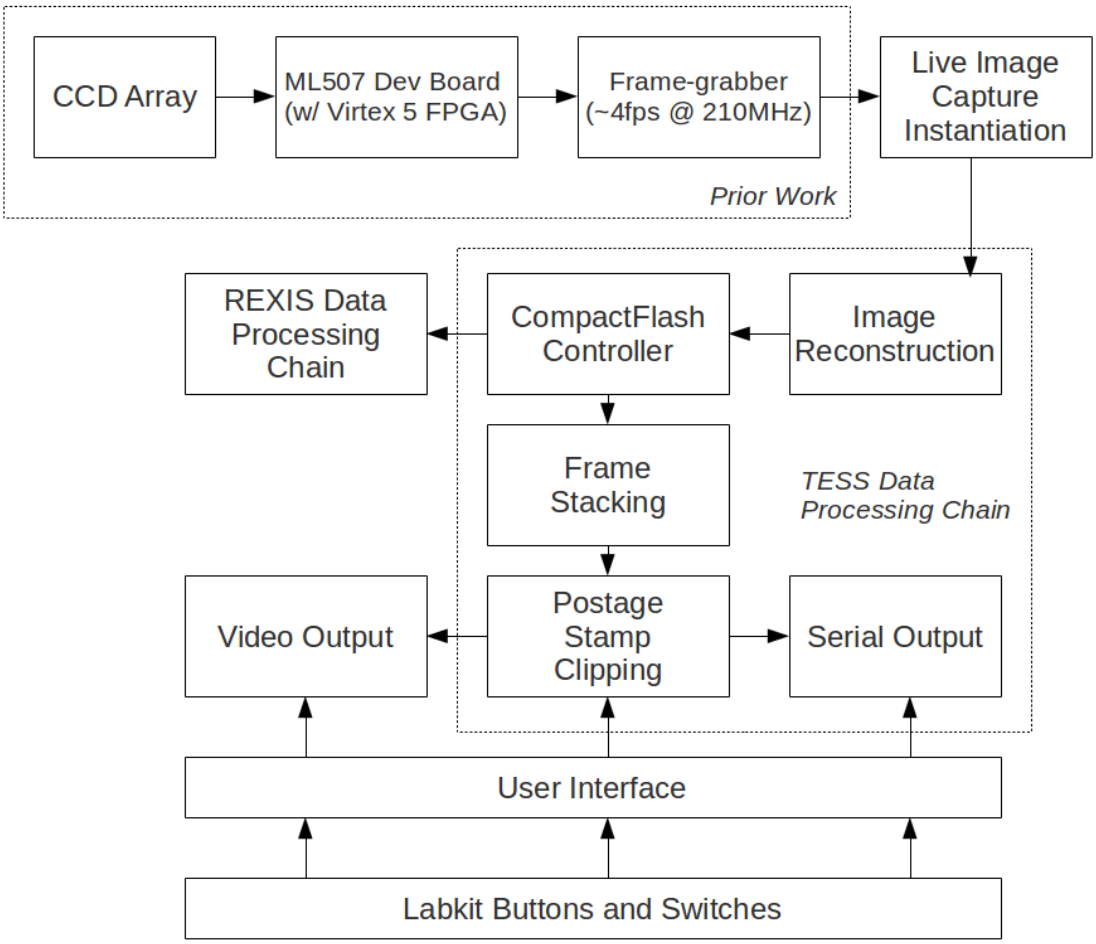

Fig. 1: System Overview Block Diagram