



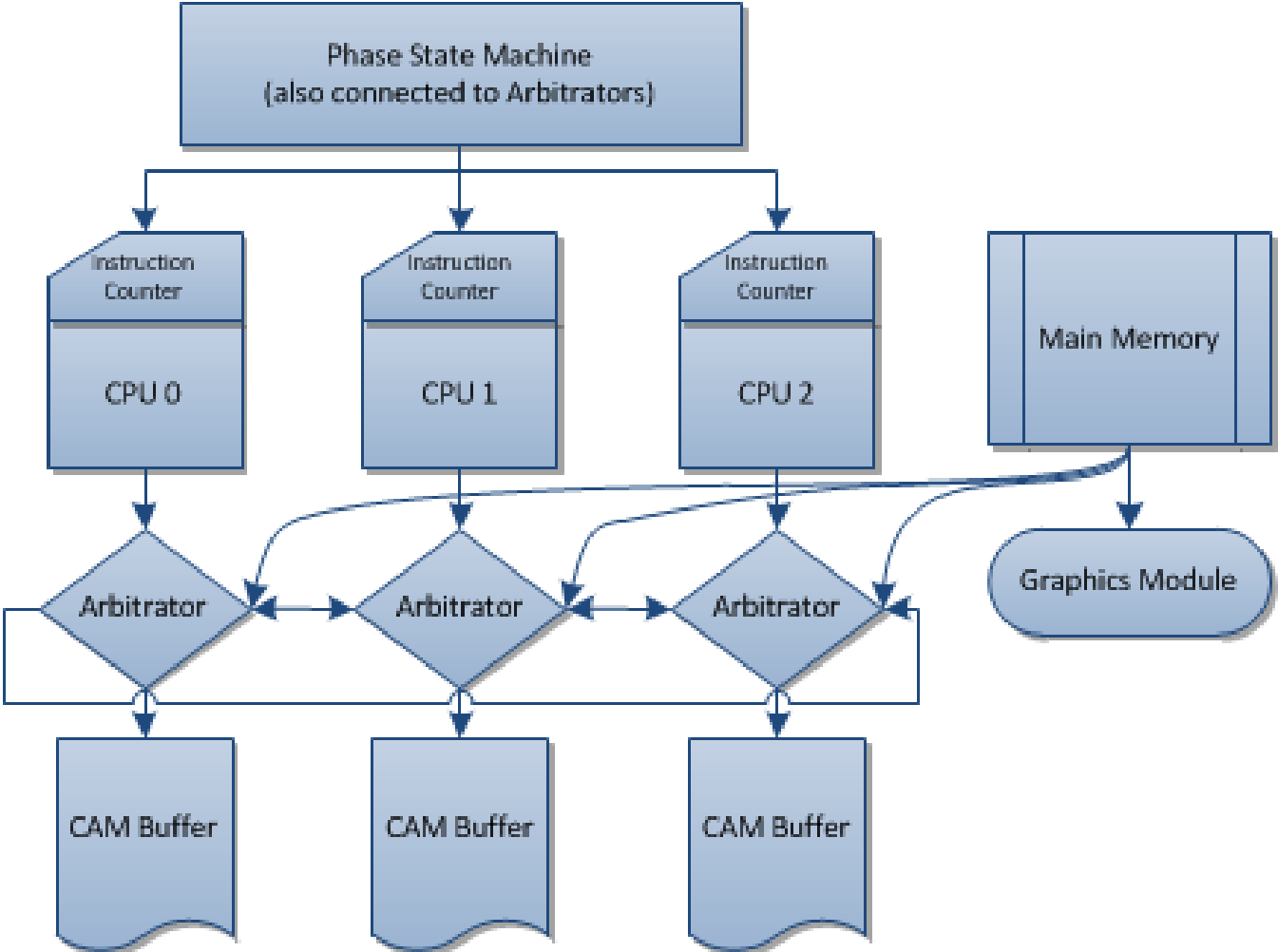
Deterministic Multiprocessing System

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Overview

- Multiprocessing is usually nondeterministic
- Nondeterminism can be removed
- Sequential Ordering
- Weak Ordering
- Build a deterministic cache for a system
 - Storage Buffers

Block Diagram



Storage Buffer

Content Addressable Memory

One read/write port

One add/remove port

Arbitrator

Commits memory during deterministic commit

Fetches new data into storage buffer

Controls CPU

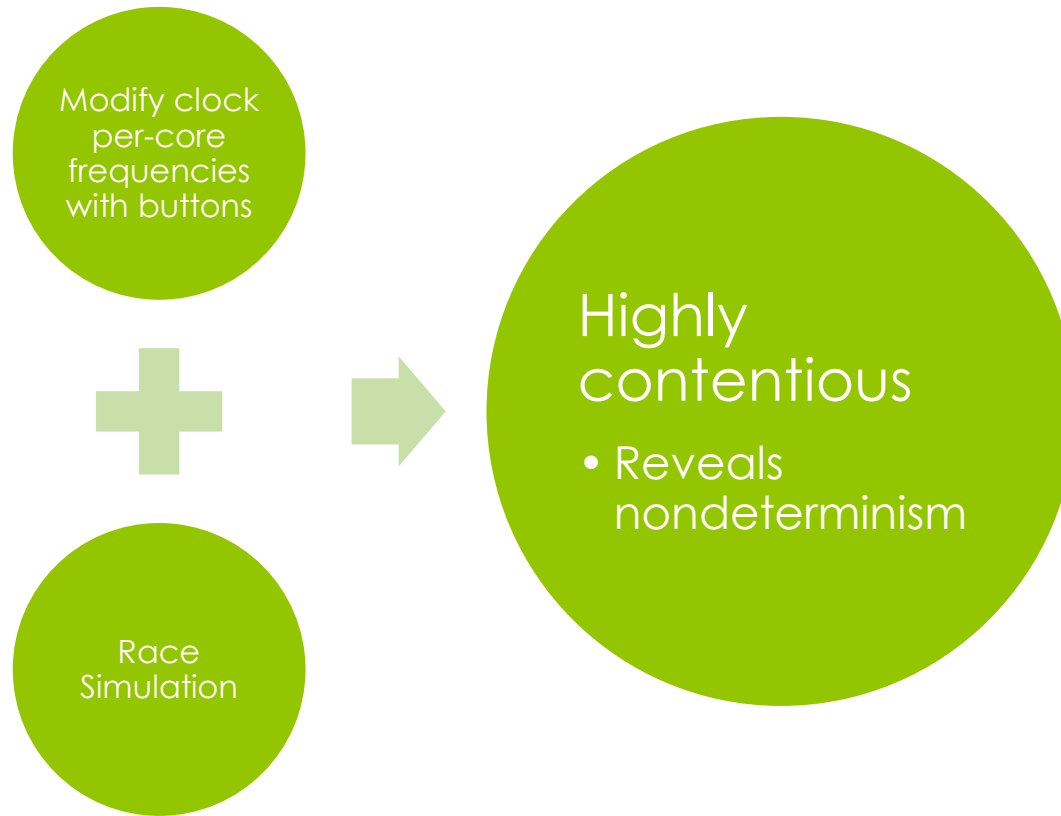
CPU, Memory, Graphics

Micro8 from
class

Modified
memory-
mapped Lab
5 graphics

BRAMS

Demo



Timeline

By 11/22 Storage
Buffer Written &
Tested

By 11/24 Arbitrator Written
& Tested

By 11/30 System
Integrated, sample code
ran

By 12/7 Debugging + final
program code written

