Deterministic Cache for a Multiprocessing System
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Multiprocessing architectures traditionally suffer from nondeterministic execution. This project seeks to implement a hardware cache system based on the work by Bergan et al. on CoreDet. The system will allow the processor to execute in parallel until interprocessor communication is detected. Then, all processors will be halted and the pending memory writes will be reordered and flushed. By deterministically reordering memory accesses, execution will appear deterministic from the perspective of the main memory without losing parallelism. The cache will be comprised of one fully associative storage buffer per processor along with an arbitration unit that will conduct the cache coherency protocol.