

## Decision-Feedback Equalizer

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The main lesson learnt through debugging of this final project was, again (yes, again), the confusion between signed and unsigned operations in Verilog. There might be possibly other reasons that a piece of Verilog code could work in ModelSim simulation but not on the Xilinx labkit. However, in our project, the only bugs were that occasionally ModelSim and Xilinx ISE seem to have different interpretation of our Verilog codes on the signed numbers and signed operations.

For example, ModelSim would have no problem with the following piece of Verilog code and simulates the desired histogram function well, while at least in this project, Xilinx would think that the last 16 cases of “in” could never occur and on the VGA output, we could only see half the histogram as all the bins for negative “in” are empty. If I replaced the “-5'd1” with “5'd31” as well as for all other negative “in” cases, the code would then work both in ModelSim simulation and on the Xilinx labkit.

```
input wire signed [4:0] in;
... ..
always @(posedge clk) begin
    ... ..
    case(in)
        5'd15: bin15 <= bin15 + 1;
        ... ..
        5'd3: bin3 <= bin3 + 1;
        5'd2: bin2 <= bin2 + 1;
        5'd1: bin1 <= bin1 + 1;
        5'd0: bin0 <= bin0 + 1;
        -5'd1: binn1 <= binn1 + 1;
        -5'd2: binn2 <= binn2 + 1;
        -5'd3: binn3 <= binn3 + 1;
        -5'd4: binn4 <= binn4 + 1;
        ... ..
        -5'd16: binn16 <= binn16 + 1;
    endcase
    ... ..
end
```

In conclusion, if BEHAVIORAL simulation works, on Xilinx labkit it does NOT necessarily work. One should have confidence that a piece of Verilog code will work on Xilinx, only if simulation on synthesized netlist works. Though, unfortunately we never did any simulation on Xilinx-synthesized netlists during the course of final project.