Training-sequence-tolerant Decision Feedback Equalizer

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On the receiver side of communication channel, decision feedback equalizer (DFE) has been widely used to cancel inter-symbol interference (ISI). In most designs, the DFE training algorithm assumes that the training-sequences are known or purely random. However, the generation mechanism of training sequence is often biased; in particular, the standard SATA training algorithm generates more zeros than ones. The training sequence heavily influences the steady state equalizer function. Training on an unexpected, or otherwise biased patterns, will cause unnecessary error. In the industry, it is most cost effective to design a general DFE for multiple applications, but because of the traditional standards set for these, the nature of the training sequence may be different from one application to another.

In this project, we will program the FPGA to act as a least-mean-square DFE and added features to account for biased training-sequences. We want to design a blind DFE that can hold simple compare-and-store data that will be able to adjust for things like: an unbalances number of 0's to 1's and other non-random behavior in the training sequence, and adjust for these such that our DFE will be able to minimize bit error. Given some input image, distorted though an ISI channel, we display the received data , with DFE or bypassing DFE, on a screen through VGA to demonstrate the effectiveness of the designed DFE.